SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF COMPUTER SCIENCE AND TECHNOLOGY

COURSE CODE & NAME : 19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR / III SEMESTER

Unit 2 : ARITHMETIC OPERATIONS

Topic : Addition and subtraction of signed numbers

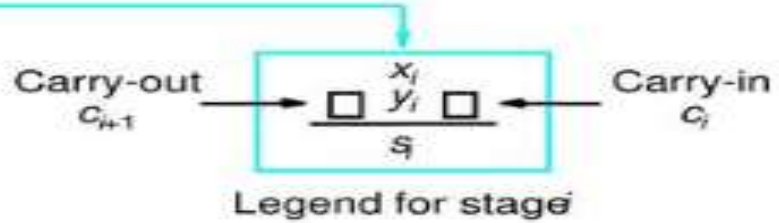
Signed Numbers

x_i	y_i	Carry-in c_i	Sums s_i	Carry-out c_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$s_i = \bar{x}_i \bar{y}_i c_i + \bar{x}_i y_i \bar{c}_i + x_i \bar{y}_i \bar{c}_i + x_i y_i c_i = x_i \oplus y_i \oplus c_i$$
$$c_{i+1} = y_i c_i + x_i c_i + x_i y_i$$

Example:

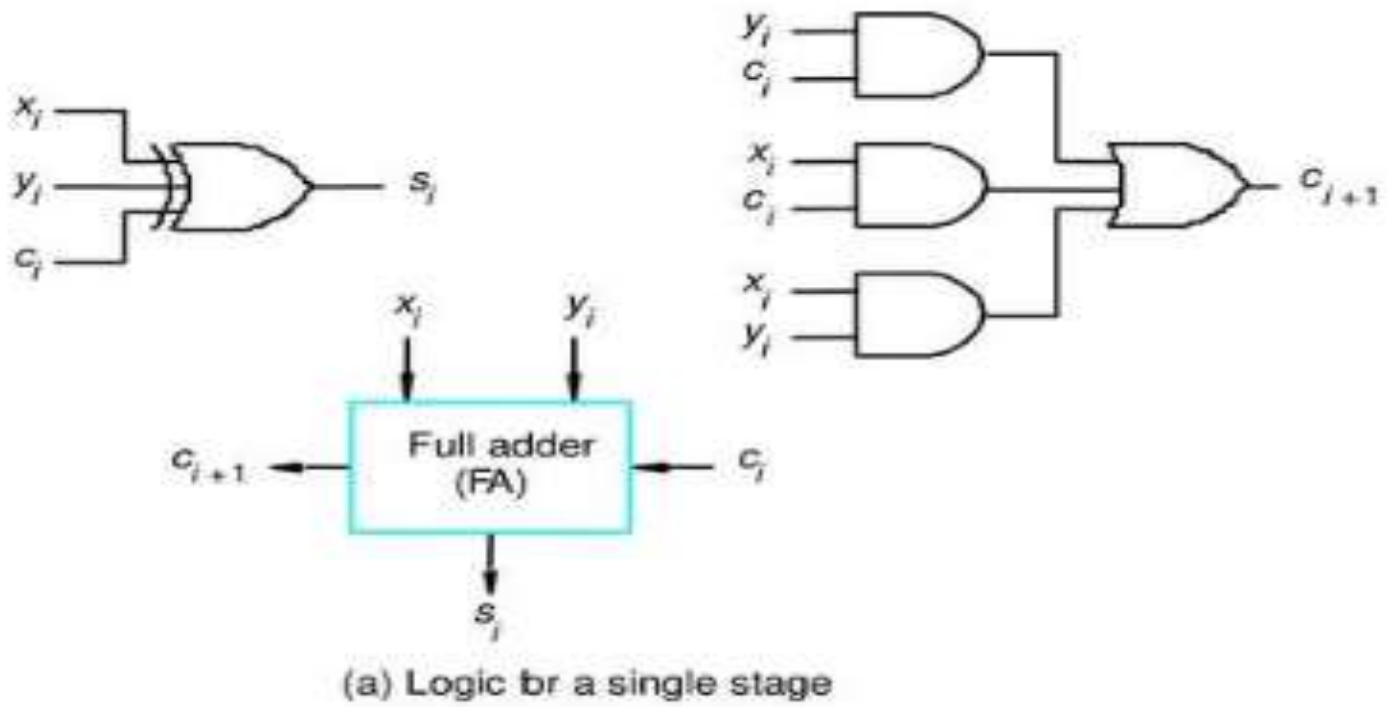
$$\begin{array}{r} X \\ +\ Y \\ \hline Z \end{array} = \begin{array}{r} 7 \\ +\ 6 \\ \hline 13 \end{array} = \begin{array}{r} 0\ 1\ 1\ 1 \\ +\ 0\ 0\ 1\ 1\ 0\ 0 \\ \hline 1\ 1\ 0\ 1 \end{array}$$



Logic specification for a stage of binary addition.

Logic for single stage

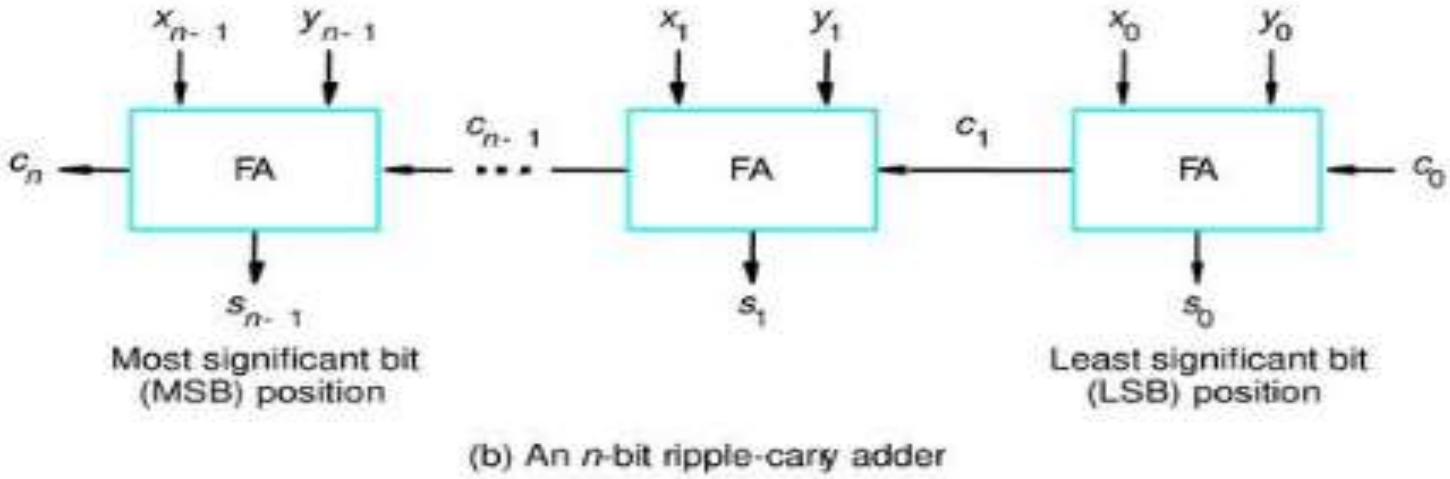
A full adder (FA)



(a) Logic br a single stage

An n-bit ripple carry adder

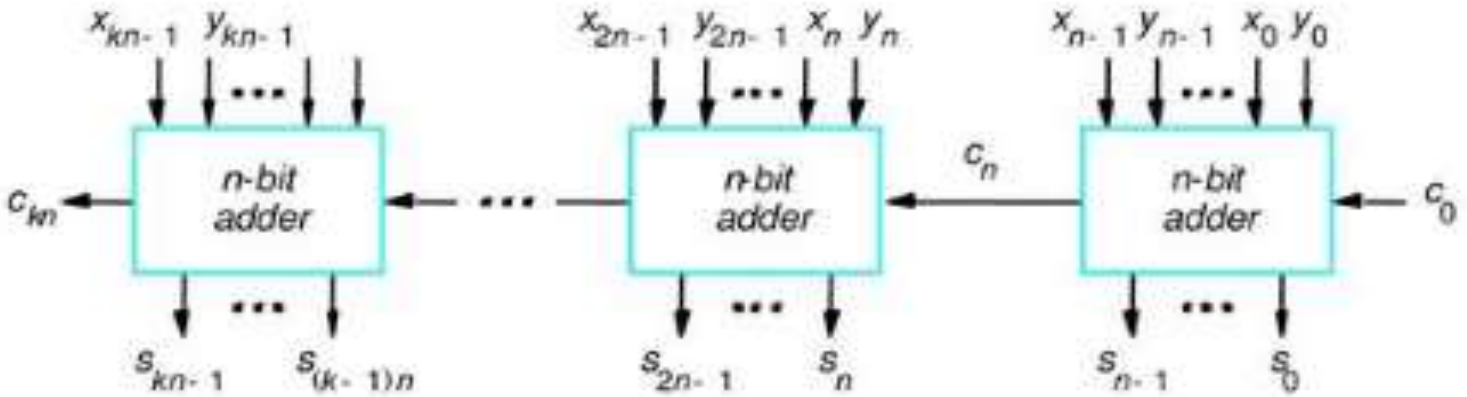
n-bit ripple-carry adder



(b) An *n*-bit ripple-cary adder

Cascade of K n-bit adders

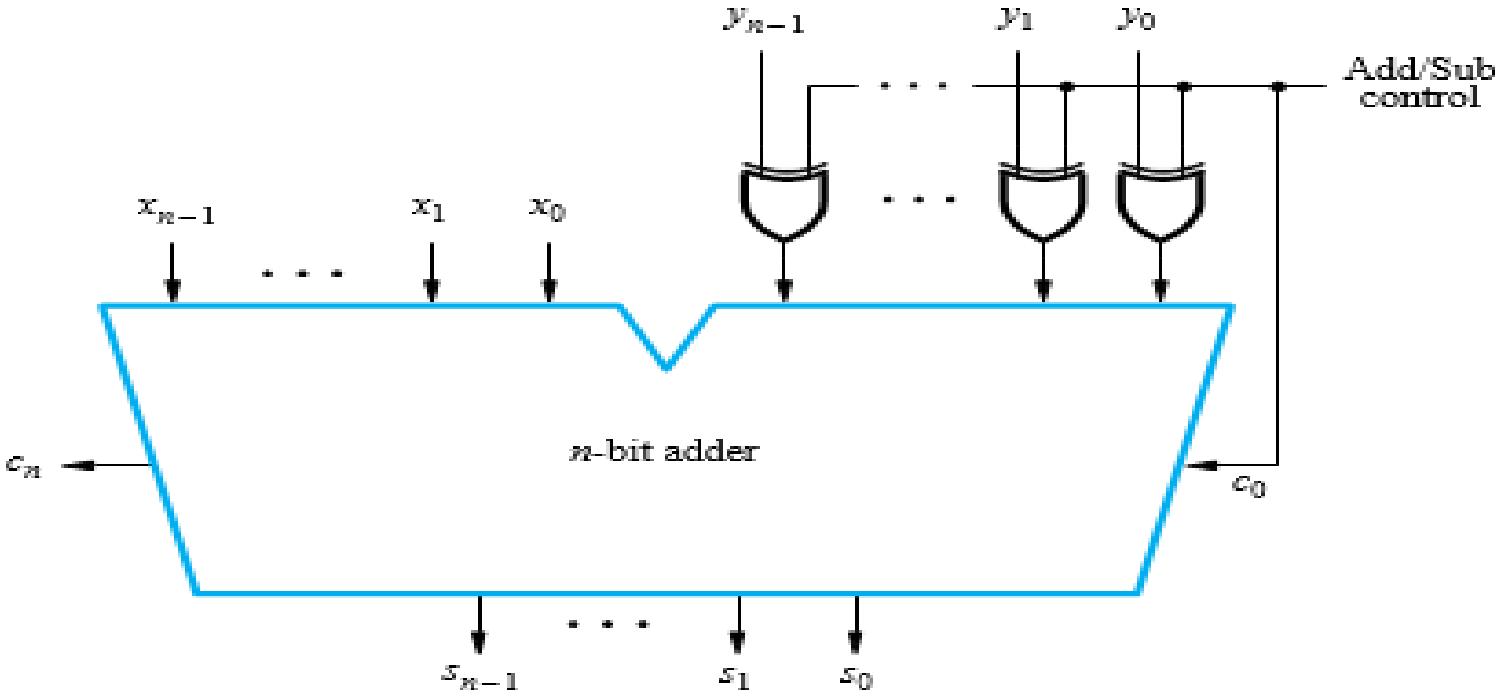
kn-bit ripple-carry adder



(c) Cascade of k *n*-bit adders

. Logic for addition of binary vectors.

Binary addition and subtraction logic circuit



Binary addition/subtraction logic circuit.

- What is Full adder?

Reference

1. Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.


Thank You!