SNS COLLEGE OF ENGINEERING

Kurumbapalayam (PO), Coimbatore – 641 107
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DEPARTMENT OF INFORMATION TECHNOLOGY

COURSE NAME: 19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR/ III SEM

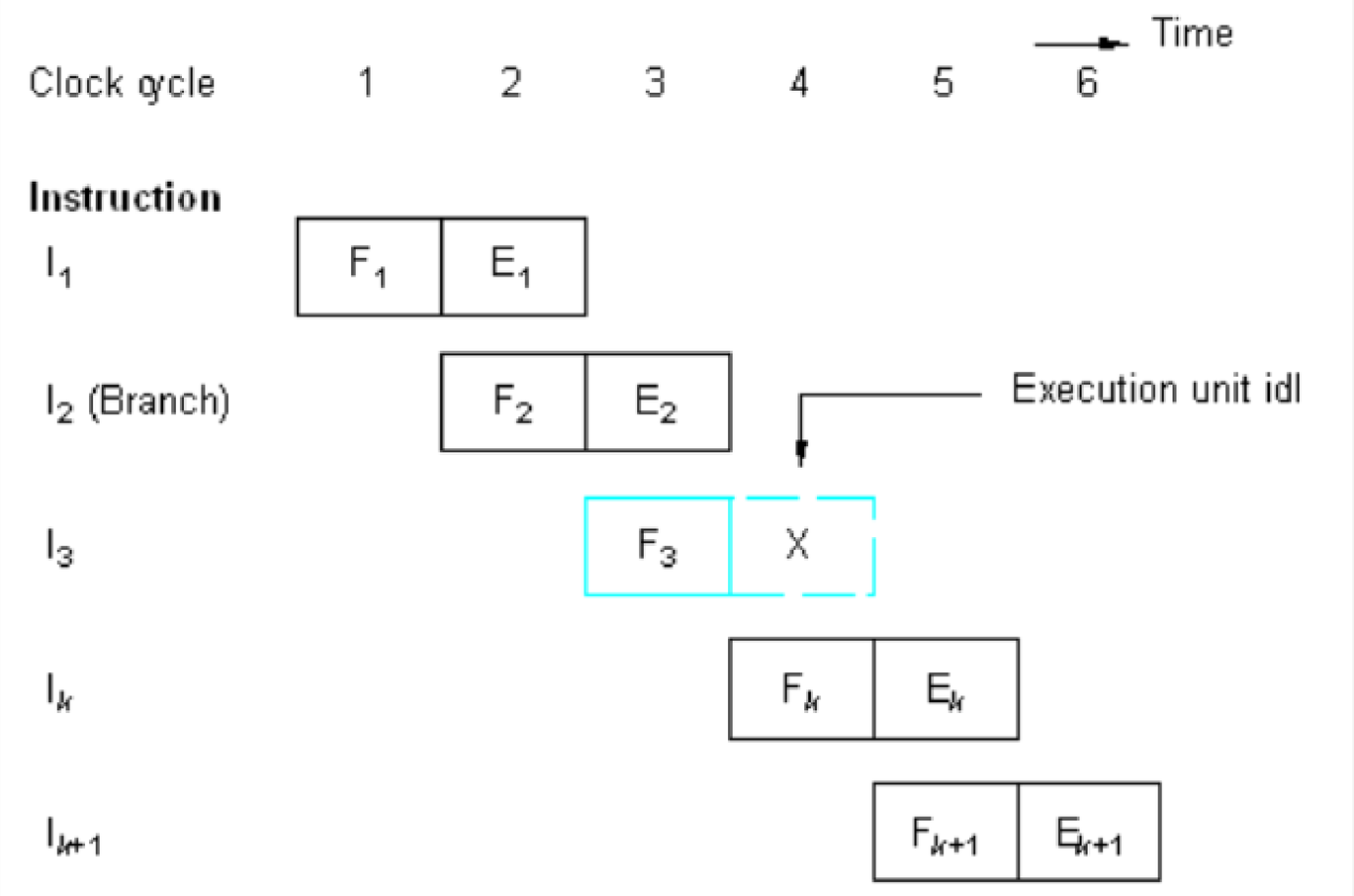
Unit 3 : Processor and Pipeling

Topic 7: Instruction Hazards

Overview – Instruction Hazards

- Whenever the stream of instructions supplied by the instruction fetch unit is interrupted, the pipeline stalls.
- Cache miss
- Branch
  - Unconditional Branches
  - Conditional branches and Branch Prediction

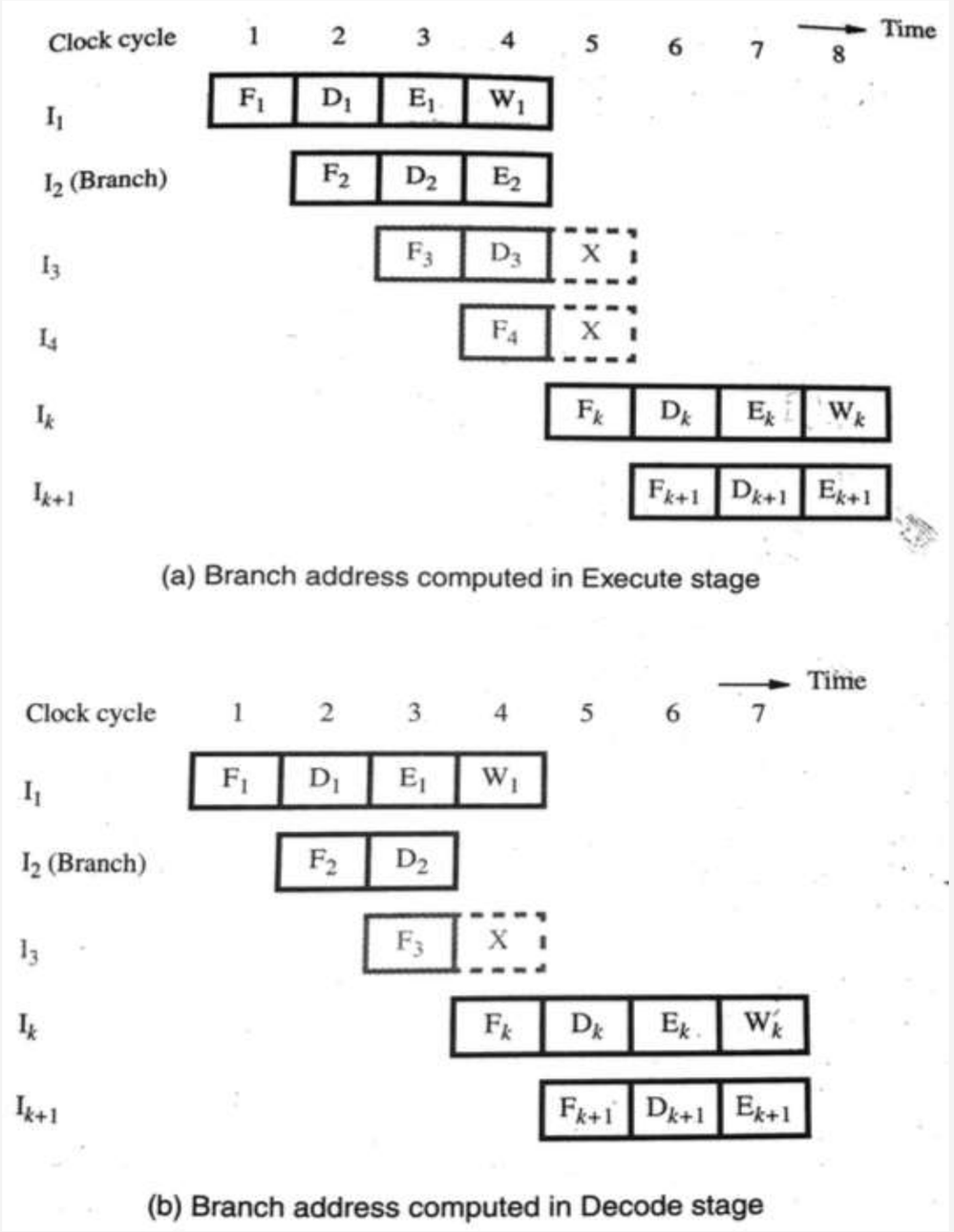
Unconditional Branches



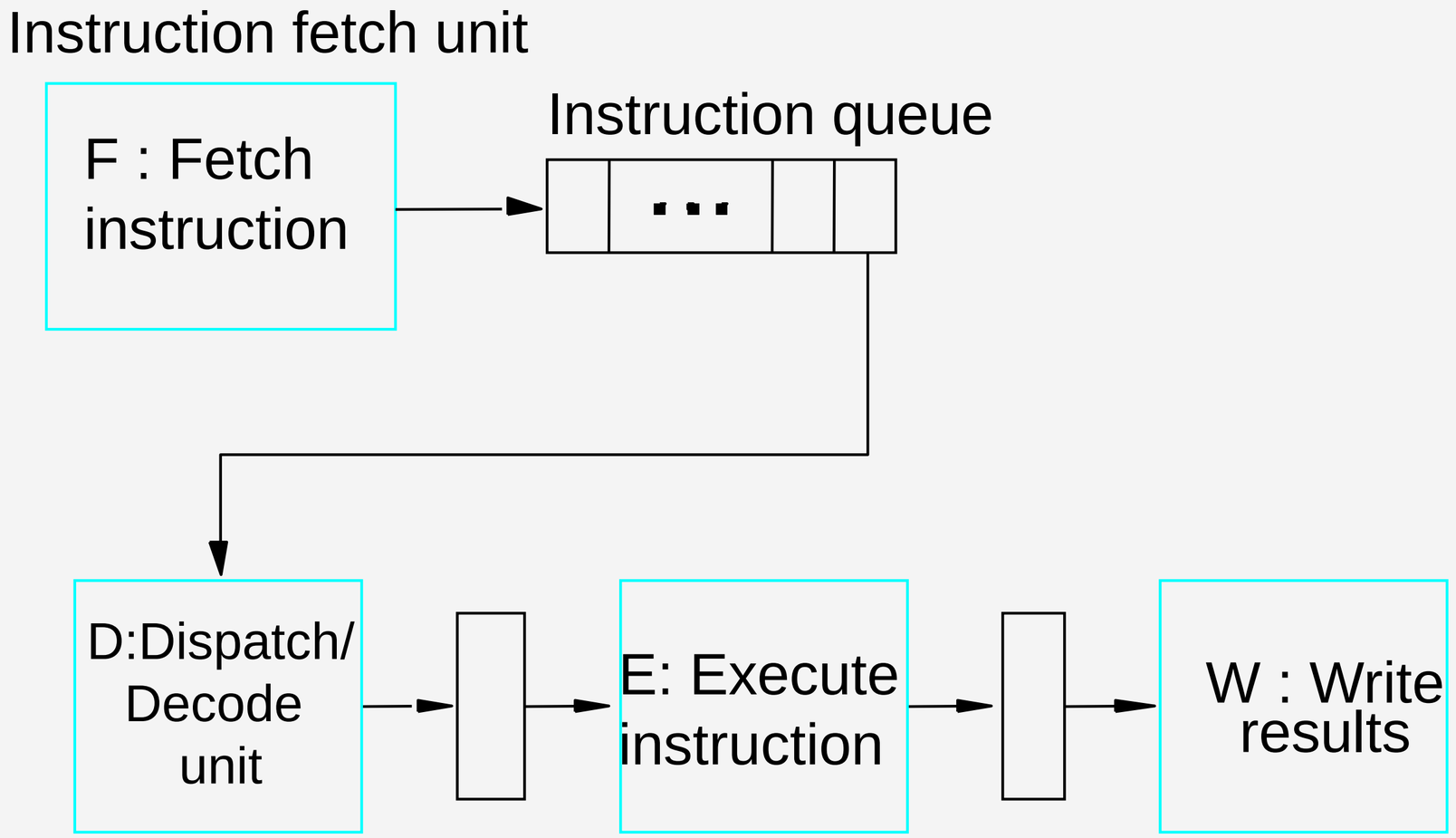
An idle cycle caused by a branch instruction

Effect of branch instruction on a four stage pipeline

- **Branch penalty:** Time lost due to branch instruction
- Reduce the penalty with additional hardware



Instruction Queue and Prefetching



Use of an instruction queue in the hardware organization

Branch Folding: Executing branch instruction concurrently with execution of other instructions

Conditional Branches

- A conditional branch instruction introduces the added hazard caused by the dependency of the branch condition
- The decision to branch cannot be made until the execution of that instruction has been completed.
- Branch instructions represent about 20% of the dynamic instruction count of most programs.
- **Dynamic count:** Number of instruction executions, taking into account the fact that some program instructions are executed many times because of loops.

Delayed Branch

- **Branch delay slot**: Instruction following the branch instruction is called a branch delay slot
- The instructions in the delay slots are always fetched. Therefore, arrange for them to be fully executed whether or not the branch is taken.
- The objective is to place useful instructions in these slots.
- The effectiveness of the delayed branch approach depends on how often it is possible to reorder instructions.

Delayed Branch

LOOP	Shift_left	R1
	Decrement	R2
	Branch=0	LOOP
NEXT	Add	R1,R3

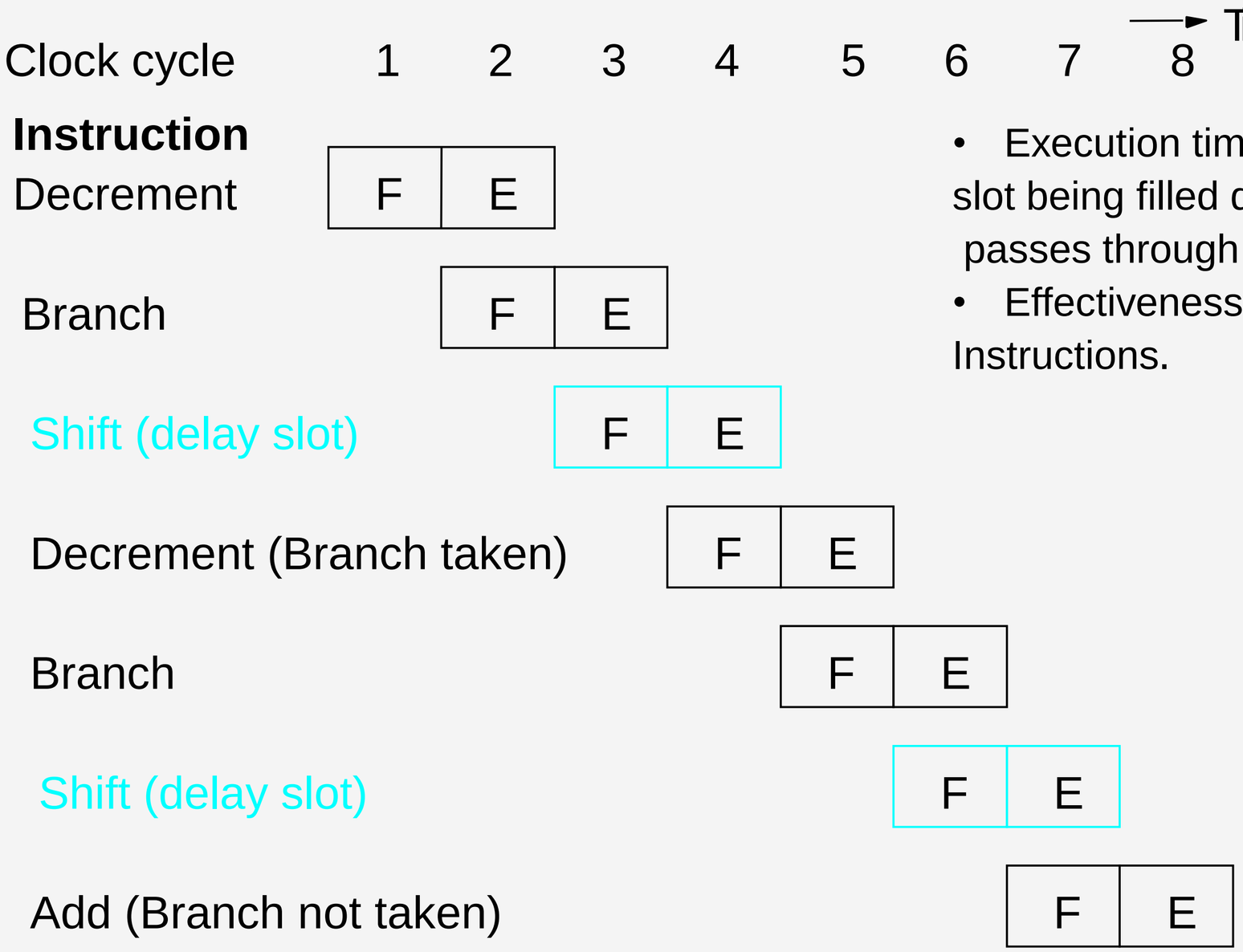
(a) Original program loop

LOOP	Decrement	R2
	Branch=0	LOOP
	Shift_left	R1
NEXT	Add	R1,R3

(b) Reordered instructions

Reordering of instructions for a delayed branch

Delayed Branch

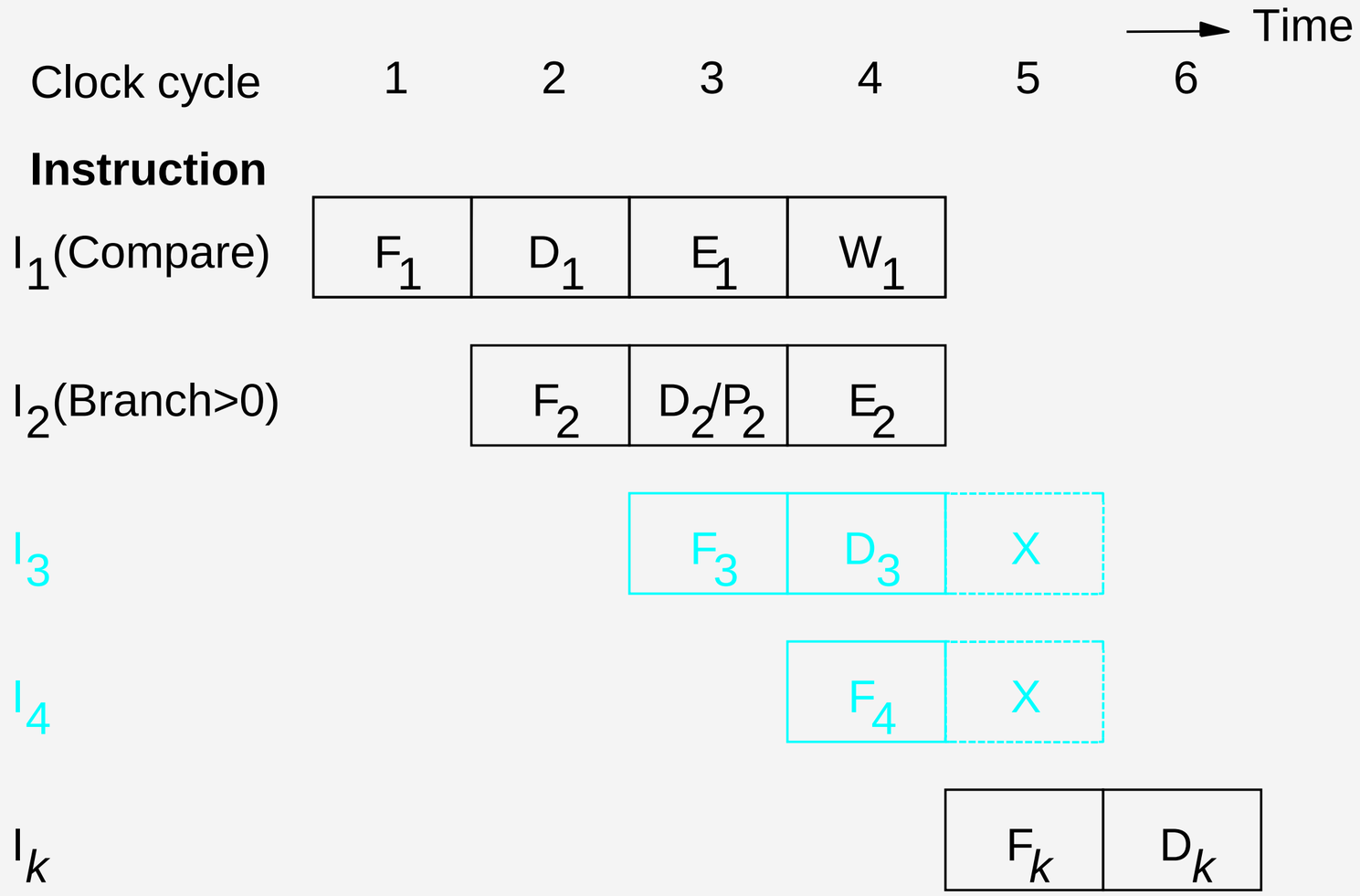


- Execution timing showing the delay slot being filled during the last two passes through the loop
- Effectiveness depends on reordering Instructions.

Branch Prediction

- To predict whether or not a particular branch will be taken.
- Simplest form: assume branch will not take place and continue to fetch instructions in sequential address order.
- Until the branch is evaluated, instruction execution along the predicted path must be done on a speculative basis.
- **Speculative execution**: instructions are executed before the processor is certain that they are in the correct execution sequence.
- Need to be careful so that no processor registers or memory locations are updated until it is confirmed that these instructions should indeed be executed.

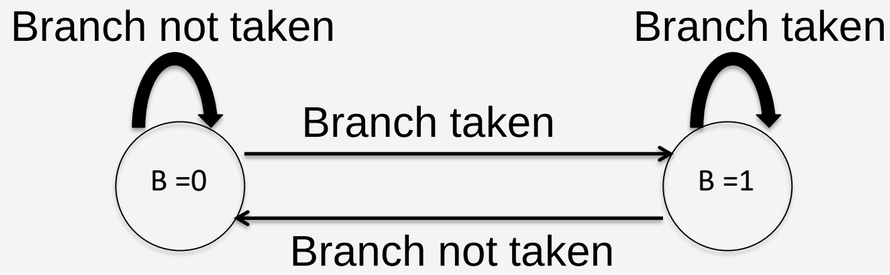
Incorrectly Predicted Branch



Timing when a branch decision has been incorrectly predicted as not taken

Branch Prediction

- Static branch prediction
  - Branch always taken
  - Branch never taken
- Dynamic branch prediction
  - Bit implementation



Gate Question

The following code is run on a pipelined processor with one delay slot.

I1: ADD R2 ⟵ R7 + R8
I2: SUB R4 ⟵ R5 – R6
I3: ADD R1 ⟵ R2 + R3
I4: STORE R4 ⟵ R1
Branch to label if R1 = = 0

Which of the instruction I1, I2, I3, I4 can legitimately occupy the delay slot without any other program modification?

a) I1 b) I2 c) I3 d) I4

Answer

d) I4

I4 could move down to branch instruction to occupy delay slot without modification in the program execution so that delay slot is effectively used due to this branch instruction

Thank You