





Kurumbapalayam (PO), Coimbatore – 641 107
Accredited by NAAC-UGC with 'A' Grade
Approved by AICTE, Recognized by UGC & Affiliated to Anna University, Chennai

#### DEPARTMENT OF INFORMATION TECHNOLOGY

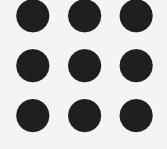
**COURSE NAME: 19IT301 COMPUTER ORGANIZATION** 

**AND ARCHITECTURE** 

II YEAR/ III SEM

**Unit 3: Processor and Pipeling** 

**Topic 3.3 - Hardwired control** 







#### Overview of Hardwired Control



- To execute instructions, the processor must have some means of generating the control signals needed in the proper sequence.
- Two categories for this purpose:
  - 1. Hardwired control
  - 2. Microprogrammed control
- Hardwired control is a method of control unit design
- The control-signals are generated by using logic circuits such as gates, flip-flops, decoders etc.





#### Overview of Hardwired Control



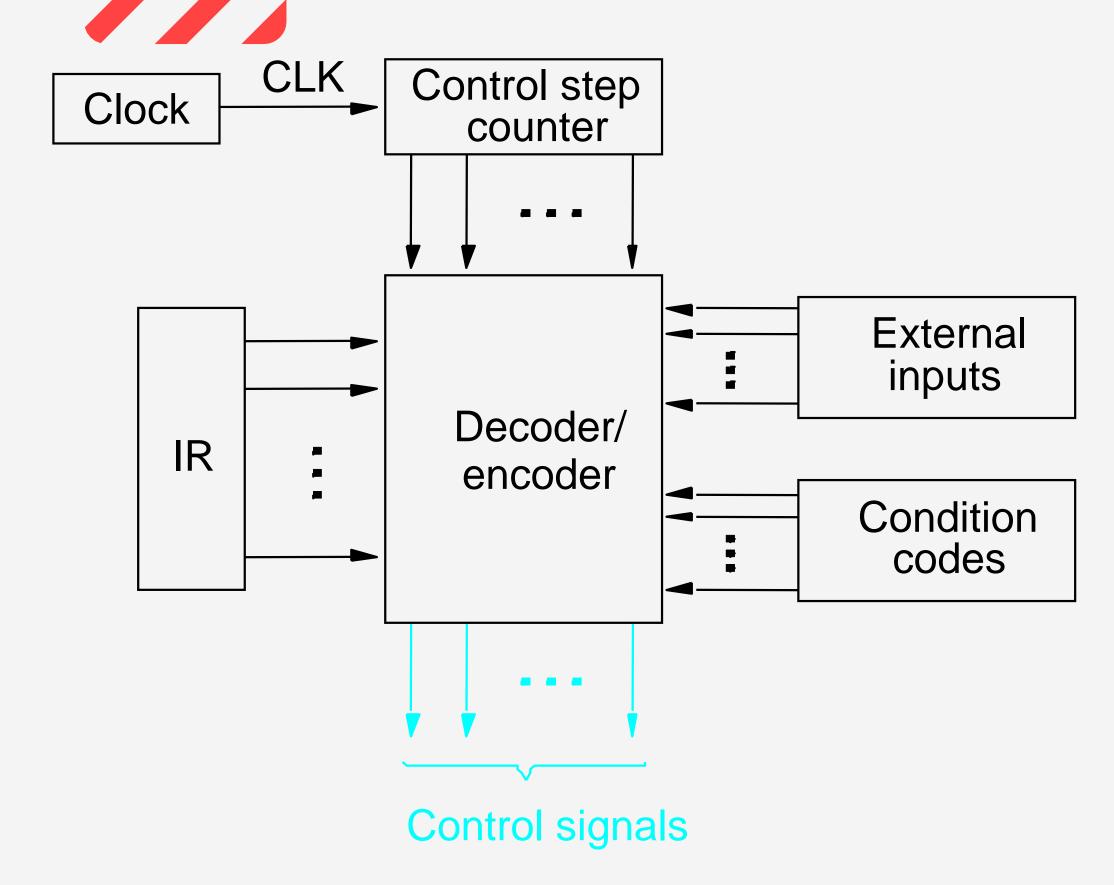
- Each step in the control sequence is completed in one clock period.
- Counter is used to keep track of control steps.
- Control signals are determined by
  - Contents of the control step counter
  - Contents of the IR
  - Contents of the condition code flags
  - External input signals like MFC and interrupt requests

Step Action	
1	PC <sub>out,</sub> MAR in, Read, Select4, Add, Zin
2	Zout, PC in, Yin WMF C
3	MDR out, IR in
4	R3 <sub>out.</sub> MAR <sub>in</sub> , Read
5	R1 <sub>out</sub> , Y <sub>in</sub> , WMFC
6	MDR <sub>out,</sub> SelectY, Add, Z <sub>in</sub>
7	Z <sub>out,</sub> R1 <sub>in</sub> , End
	Control Sequence



# Control Unit Organization

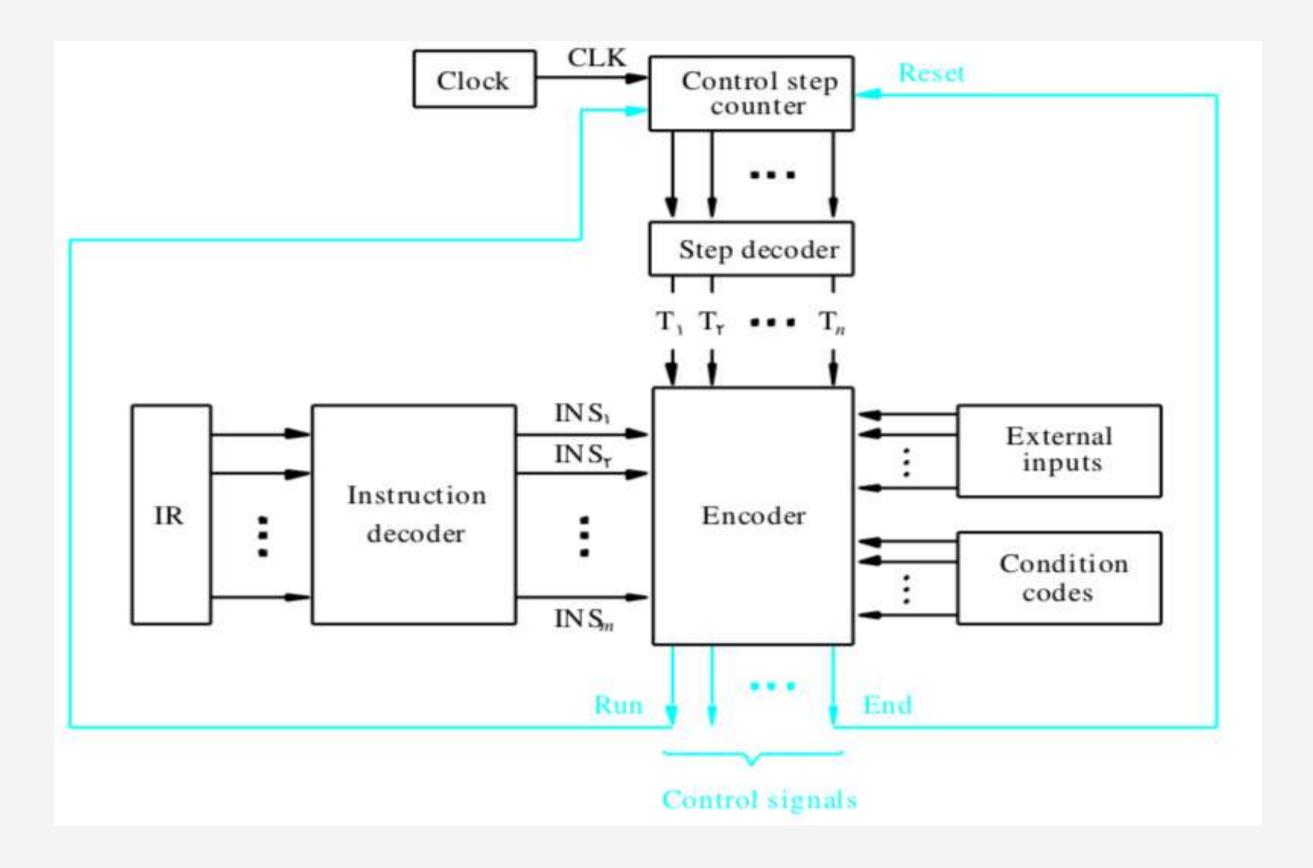






### Detailed Block Description





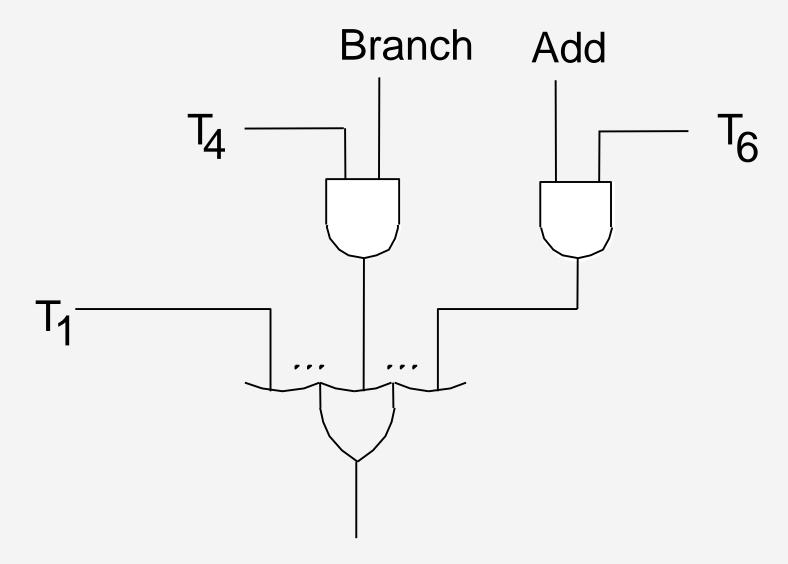




## Generating Z<sub>in</sub>



$$Z_{in} = T_1 + T_6 \cdot ADD + T_4 \cdot BR + \dots$$





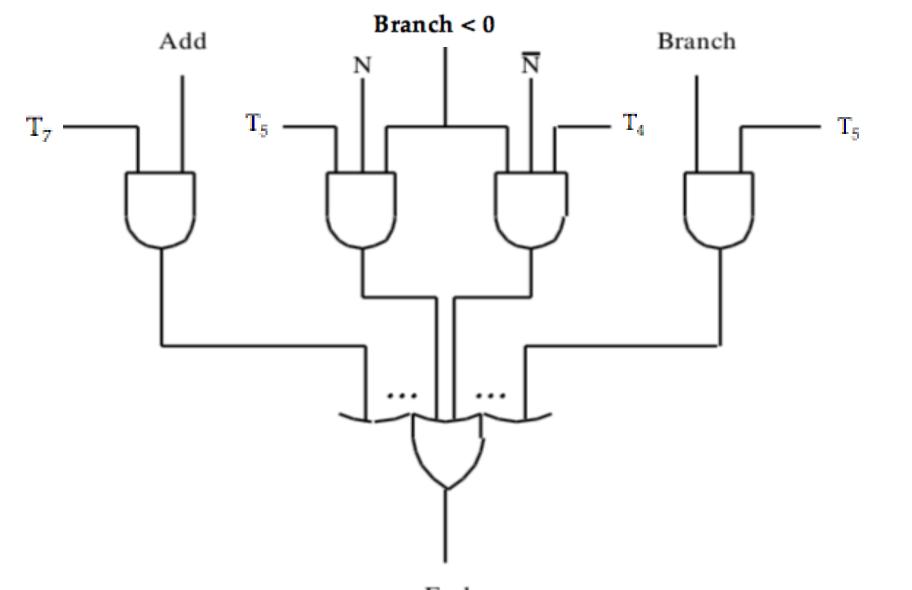




### Generating End



End =  $T_7 \cdot ADD + T_5 \cdot BR + (T_5 \cdot N + T_4 \cdot N) \cdot BRN + ...$ 

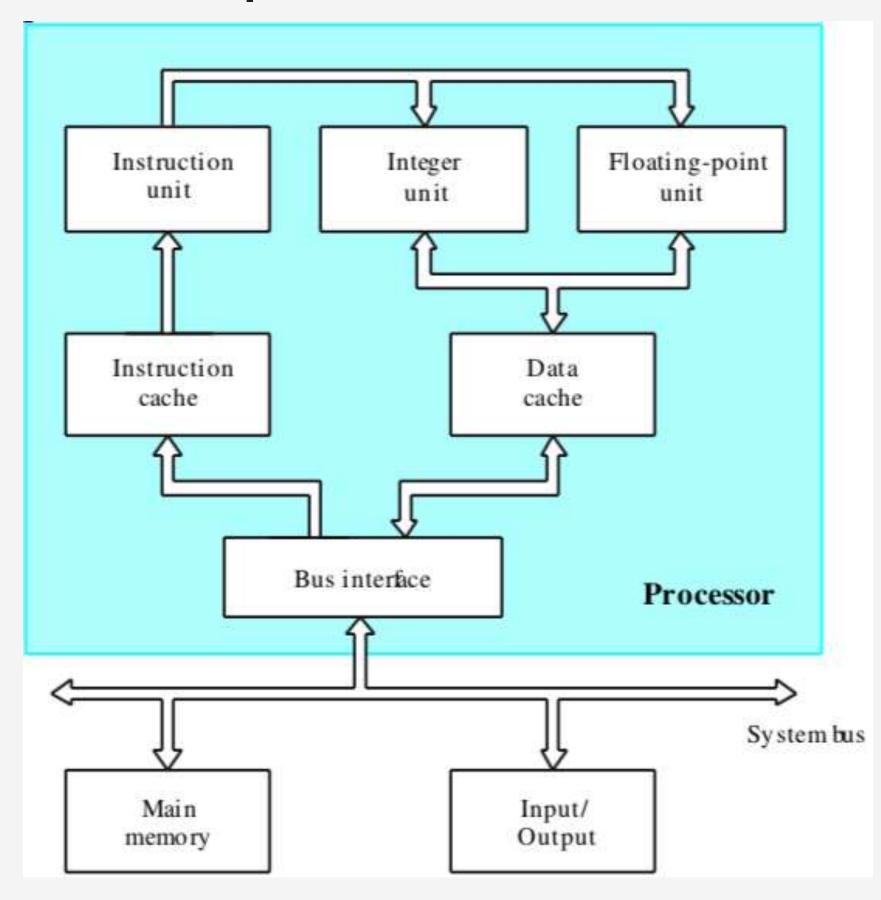


- Sequence of operation is determined by wiring of the logic elements hence the name 'hardwired'
- Hardwired system can operate at high speed; but with little flexibility.
   SNSCE / IT / V Sem / V. Vaishnavee AP-IT



# Complete Processor





SNSCE / IT/ V Sem/V.VaishnaveeAP-IT





#### Thank You