SNS COLLEGE OF ENGINEERING

Kurumbapalayam (PO), Coimbatore – 641 107
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DEPARTMENT OF INFORMATION TECHNOLOGY

COURSE NAME: 19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR/ III SEM

Unit 2 : ARITHMETIC OPERATIONS

Topic 5: Fast Multiplication

Fast Multiplication

Two techniques for speeding up the multiplication operation

1. Bit-pair Recoding of Multipliers
2. Carry-Save addition of summands

Bit-pair Recoding of Multipliers:

- Guarantees the maximum number of summands (versions of multiplicand) added is n/2 for n-bit operands

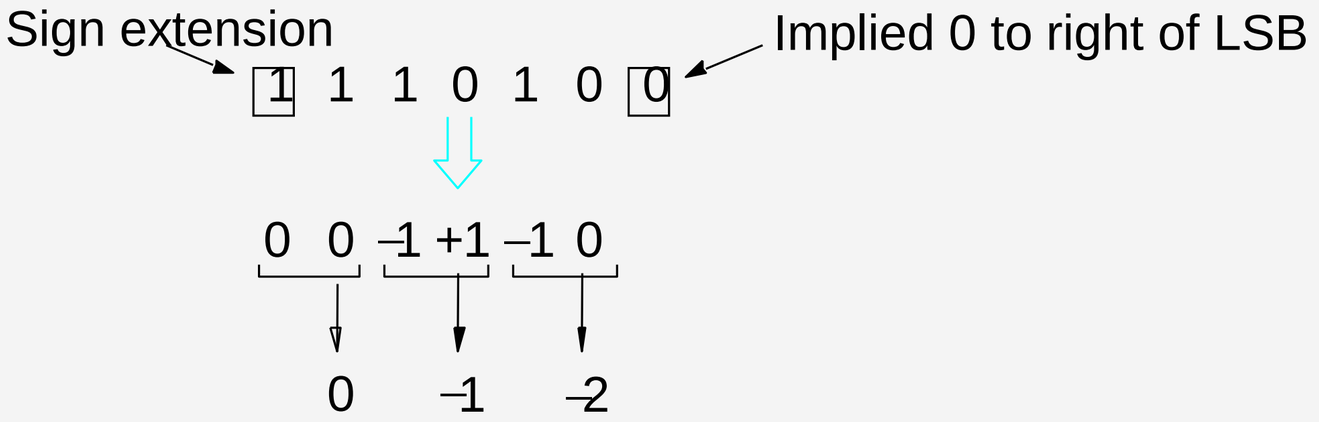
Carry-Save Addition of summands

- Reduces the time needed to add the summands

Bit-pair Recoding of Multipliers

- It halves the maximum number of summands
- Derived from Booth algorithm

Multiplier		Version of multiplicand selected by bit *i*
Bit*i*	Bit*i*-1	
0	0	0 X M
0	1	+1 X M
1	0	–1 X M
1	1	0 X M



Example of bit-pair recoding derived from Booth recoding

Multiplier Bit pair recoding

Multiplier bit-pair		Multiplier bit on the right	Multiplicand selected at position *i*
i + 1	*i*	*i* – 1	
0	0	0	0 X M
0	0	1	+ 1 X M
0	1	0	+ 1 X M
0	1	1	+ 2 X M
1	0	0	– 2 X M
1	0	1	– 1 X M
1	1	0	– 1 X M
1	1	1	0 X M

Table of multiplicand selection decisions

Example: Booth Multiplication

0	1	1	0	1	(+13)
1	1	0	1	0	(- 6)

-13 = 1 0 0 1 1

					0	1	1	0	1	
					0	-1	+1	-1	0	
0	0	0	0	0	0	0	0	0	0	
1	1	1	1	1	0	0	1	1		
0	0	0	0	1	1	0	1			
1	1	1	0	0	1	1				
0	0	0	0	0	0					
1	1	1	0	1	1	0	0	1	0	(- 78)

Example

Multiplier: 11010

1 1 0 1 0 0

0 -1 -2

+13 = 0 1 1 0 1

1's = 1 0 0 1 0

2's = 1 +

-13 = 1 0 0 1 1

-1 = 2's complement of multiplicand

-2 = 2's complement of multiplicand x 1 0

+1 = Multiplicand

+2 = Multiplicand x 10

Multiplicand: 0 1 1 0 1

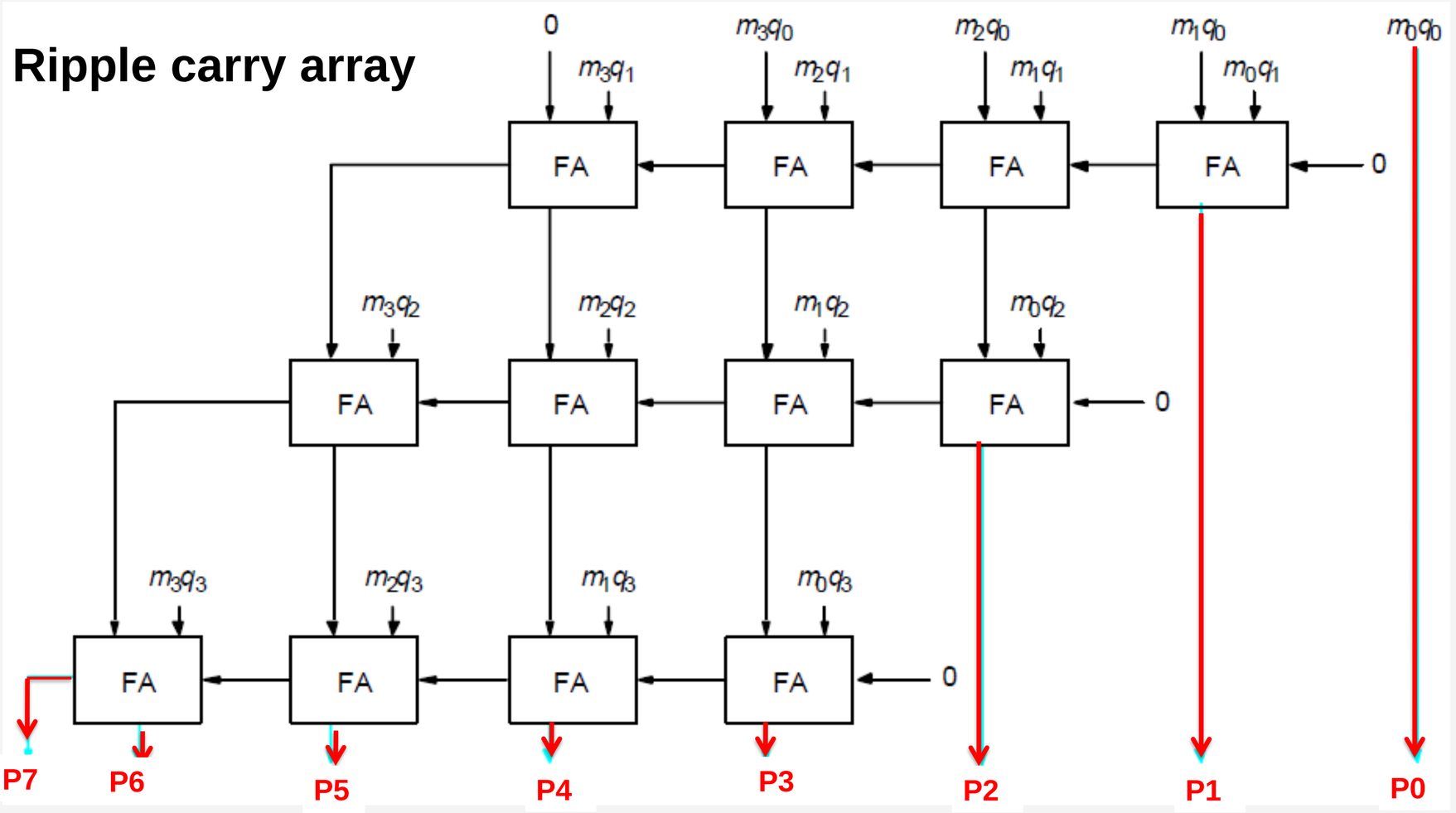
0 -1 -2

1	1	1	1	1	0	0	1	1	0
1	1	1	1	0	0	1	1	x	x
0	0	0	0	0	0	x	x	x	x
1	1	1	0	1	1	0	0	1	0

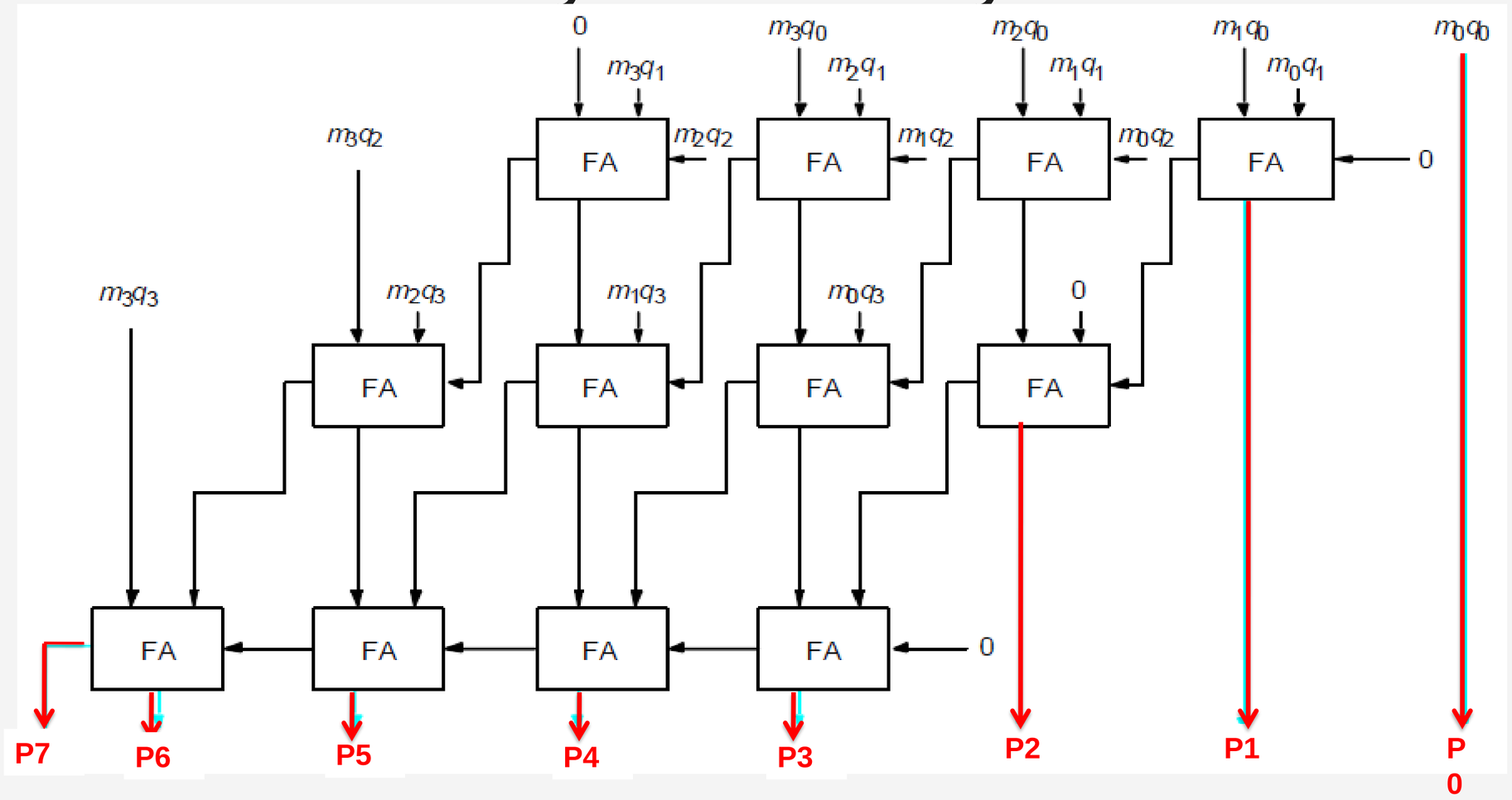
Multiplication requiring only *n*/2 summands

Carry-Save Addition of Summands

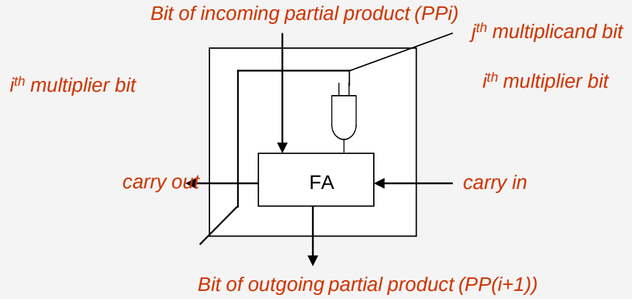
- Multiplication requires addition of several summands.
- Carry- Save Addition(CSA) technique speeds up the addition process



Carry-Save Array



M x Q = P for 4-bit operands



Carry-Save Addition of Summands

- Consider the addition of many summands, we can:
  - ➢ Group the summands in threes and perform carry-save addition on each of these groups in parallel to generate a set of S and C vectors in one full-adder delay
  - ➢ Group all of the S and C vectors into threes, and perform carry-save addition on them, generating a further set of S and C vectors in one more full-adder delay
  - ➢ Continue with this process until there are only two vectors remaining
  - ➢ They can be added in a RCA or CLA to produce the desired product

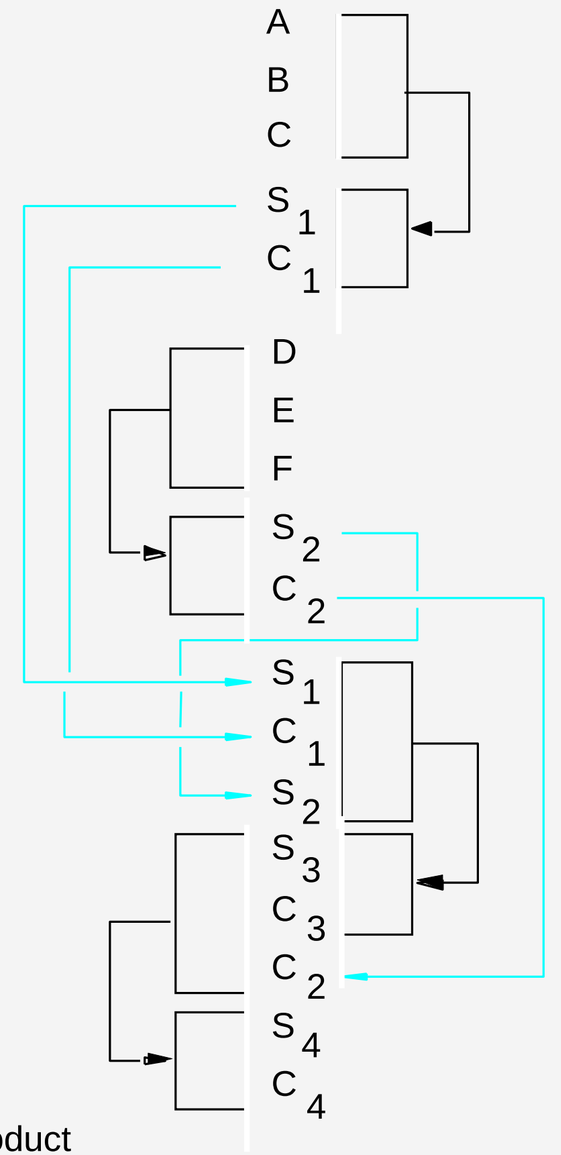
Carry-Save Addition of Summands

						1	0	1	1	0	1	(45)	M
					x	1	1	1	1	1	1	(63)	Q
m_5q_0	m_4q_0	m_3q_0	m_2q_0	m_1q_0	m_0q_0		1	0	1	1	0	1	A
m_5q_1	m_4q_1	m_3q_1	m_2q_1	m_1q_1	m_0q_1	1	0	1	1	0	1		B
				1	0	1	1	0	1				C
			1	0	1	1	0	1					D
		1	0	1	1	0	1						E
	1	0	1	1	0	1							F
1	0	1	1	0	0	0	1	0	0	1	1	(2,835)	Product

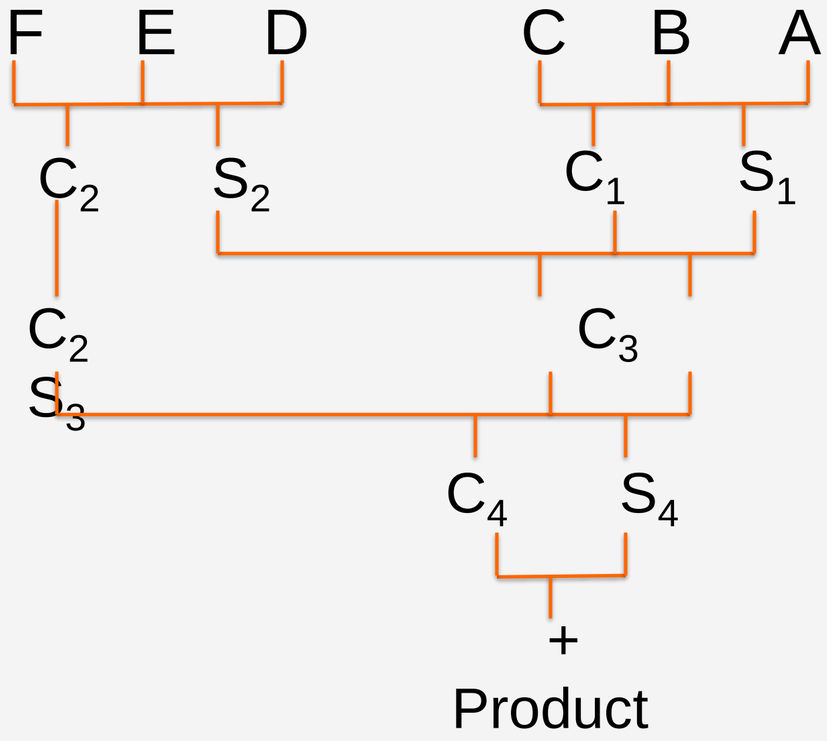
A multiplication example used to illustrate carry-save addition

Carry- Save Addition

						1	0	1	1	0	1	M
					x	1	1	1	1	1	1	Q
					1	0	1	1	0	1		
				1	0	1	1	0	1			
			1	1	0	0	0	0	1	1		
		0	0	1	1	1	1	0	0			
			1	0	1	1	0	1				
		1	0	1	1	0	1					
	1	0	1	1	0	1						
	1	1	0	0	0	0	1	1				
0	0	1	1	1	1	0	0					
				1	1	0	0	0	0	1	1	
			0	0	1	1	1	1	0	0		
	1	1	0	0	0	0	1	1				
	1	1	0	1	0	1	0	0	0	1	1	
0	0	0	0	1	0	1	1	0	0	0		
0	0	1	1	1	1	0	0					
0	1	0	1	1	1	0	1	0	0	1	1	
+ 0	1	0	1	0	1	0	0	0	0	0		
1	0	1	1	0	0	0	1	0	0	1	1	Product



Schematic Representaion of CSA



Level 1 CSA

Level 2 CSA

Level 3 CSA

Final Addition

Gate Delays

Logic gate delay to perform 6 x 6 multiplication

- 1 AND gate delay
- 2 gate delays per CSA level
- CLA has 8 gate delays

Total gate delays = 1 + 2 x 3 CSA levels + 8

= 15

In general, for n summands of n x n multiplication,

= $1.7\log_2 n - 1.7$ levels of CSA steps needed

Using bit-pair recoding,

= $1.7\log_2 n - 3.4$ levels of CSA steps needed

Assessment

1. We make use of _____ circuits to implement multiplication.
a) Flip flops
b) Combinatorial
c) Fast adders
d) None of the mentioned

2. The method used to reduce the maximum number of summands by half is _____
a) Fast multiplication
b) Bit-pair recoding
c) Quick multiplication
d) None of the mentioned

Assessment

3. The multiplier -6(11010) is recorded as _____

a) 0-1-2
b) 0-1+1-10
c) -2-10
d) None

4. CSA stands for?

a) Computer Speed Addition
b) Carry Save Addition
c) Computer Service Architecture
d) None of the mentioned

5. The product of -13 & 11 is

_____

a) 1100110011
b) 1101110001
c) 1010101010
d) 1111111000

Answers

1. C
2. B
3. A
4. B
5. B

Thank You