SNS COLLEGE OF ENGINEERING

Kurumbapalayam (PO), Coimbatore – 641 107
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DEPARTMENT OF INFORMATION TECHNOLOGY

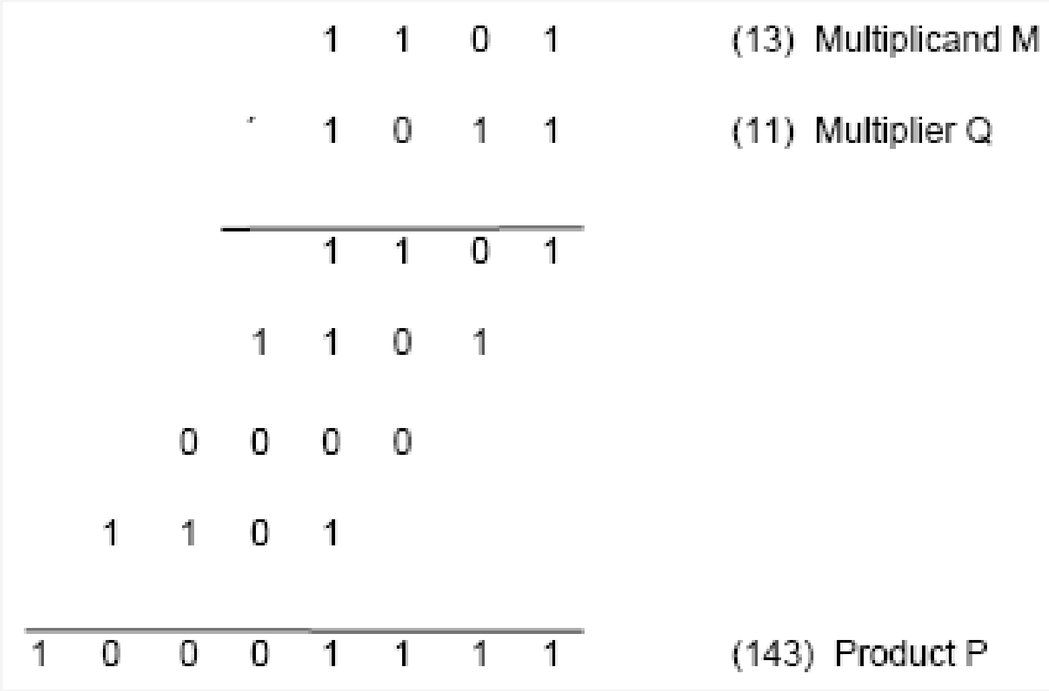
COURSE NAME: 19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR/ III SEM

Unit 2 : ARITHMETIC OPERATIONS

Topic 3: Multiplication of positive numbers

Multiplication of positive numbers



- Product of 2 n-bit numbers have 2n digits
- Unsigned multiplication can be viewed as addition of shifted versions of the multiplicand.

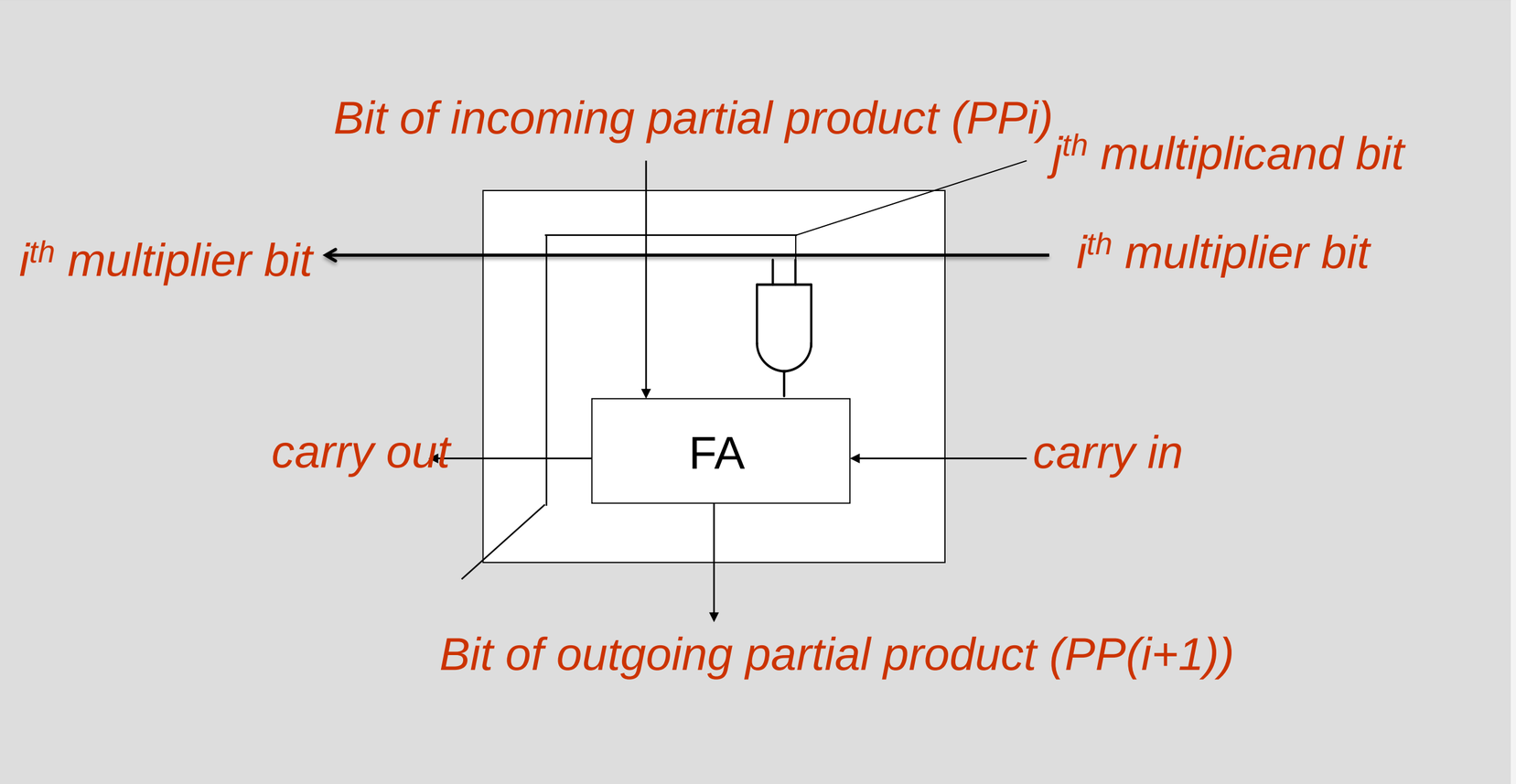
Multiplication of positive numbers

Rules to implement multiplication are:

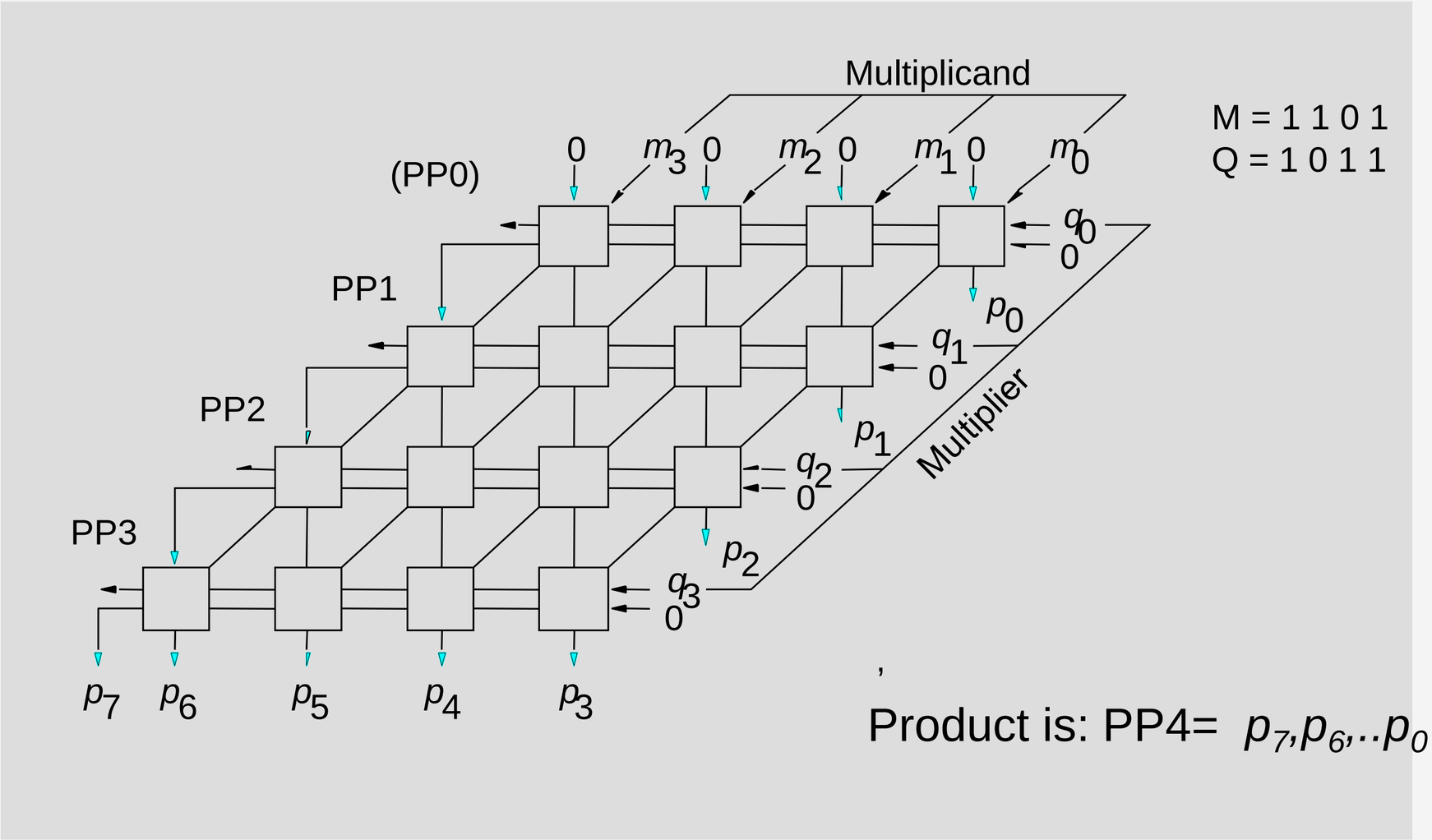
- If the i^{th} bit of the multiplier is 1, shift the multiplicand and add the shifted multiplicand to the current value of the partial product.
- Hand over the partial product to the next stage
- Value of the partial product at the start stage is 0.

Multiplication of positive numbers

Typical multiplication cell



Combinational 2D logic array



Multiplicand is shifted by displacing it through an array of adders.

Multiplication of positive numbers

Combinatorial array multipliers are:

- Extremely inefficient.
- Have a high gate count for multiplying numbers of practical size such as 32-bit or 64-bit numbers.
- Perform only one function, namely, unsigned integer product.

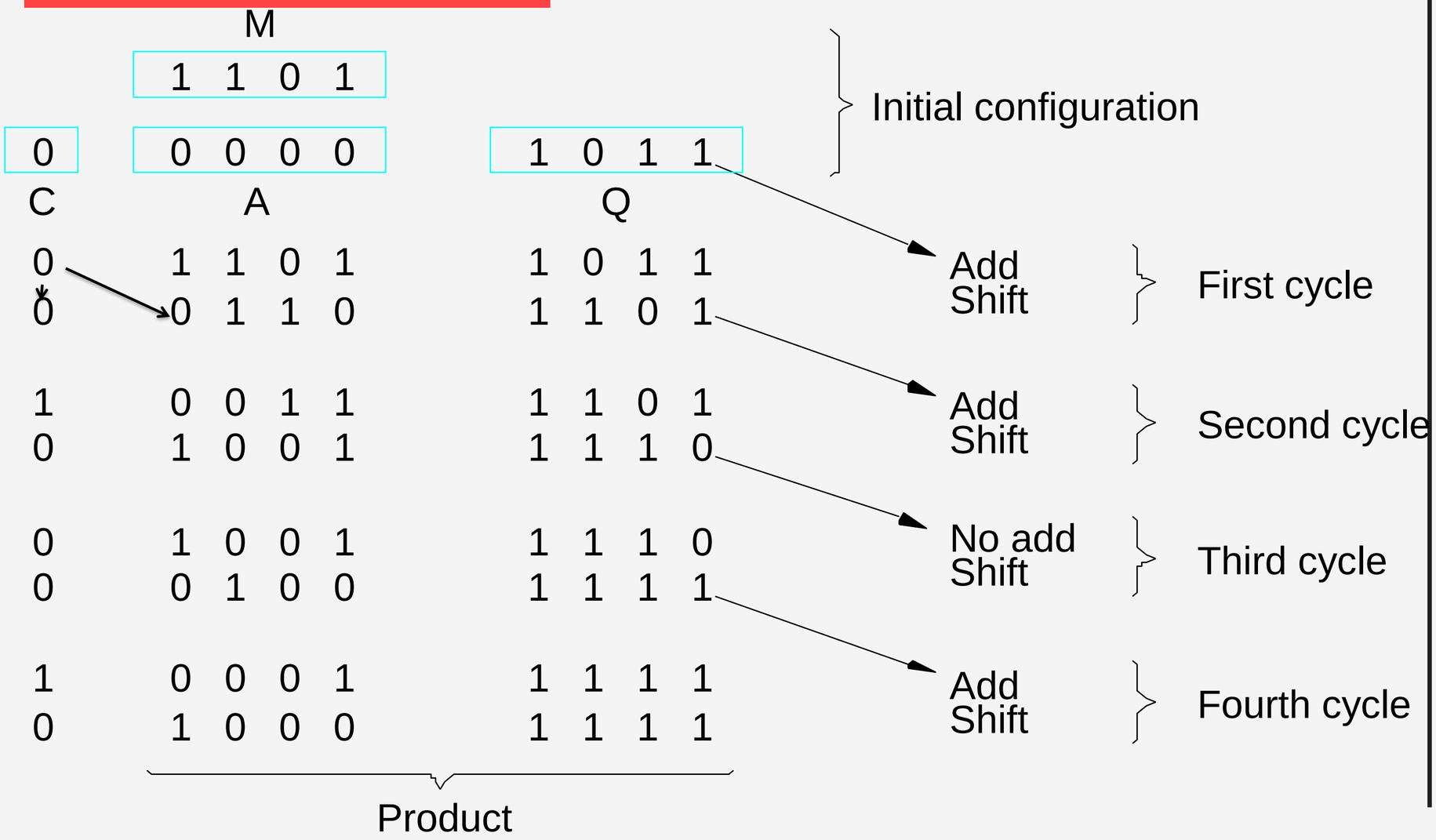
Improve gate efficiency by using a mixture of combinatorial array techniques and sequential techniques requiring less combinational logic.

Sequential multiplication

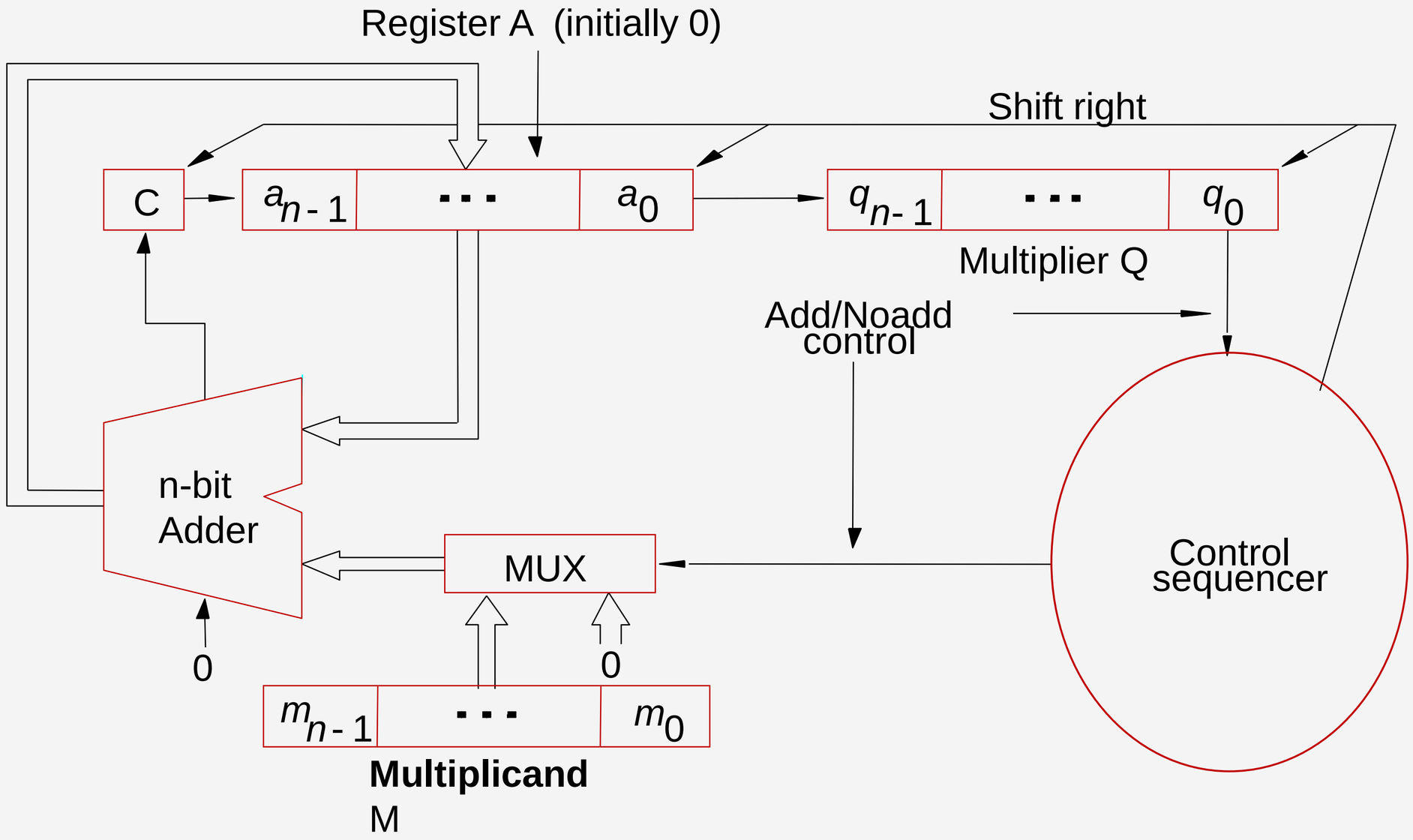
Recall the rule for generating partial products:

- If the i^{th} bit of the multiplier is 1, add the appropriately shifted multiplicand to the current partial product.
- Multiplicand has been shifted left when added to the partial product.

Sequential multiplication (contd..)



Sequential Circuit Multiplier



Disadvantage of Sequential hardware structure

- Multiply instruction takes more time to execute
- Several techniques used to speed up multiplication

Thank You