SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

II YEAR / III SEMESTER

Unit III- SEQUENTIAL CIRCUITS
Topic : Modulo n Counters

Modulus Counter (MOD-N Counter)

The 2-bit counter is called as MOD-4 counter and 3-bit counter is called as MOD-8 counter. So in general, an n-bit counter is called as modulo-N counter. Where, MOD number = 2n.

- 2-bit up or down (MOD-4)
- 3-bit up or down (MOD-8)
- 4-bit up or down (MOD-16)

Design Synchronous MOD-6 Counter Using JK flip flop

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$.

Here $N = 6$ $\therefore n = 3$

i.e. Three flip-flops are required.

Step 2 : Write an excitation table for JK flip-flop.

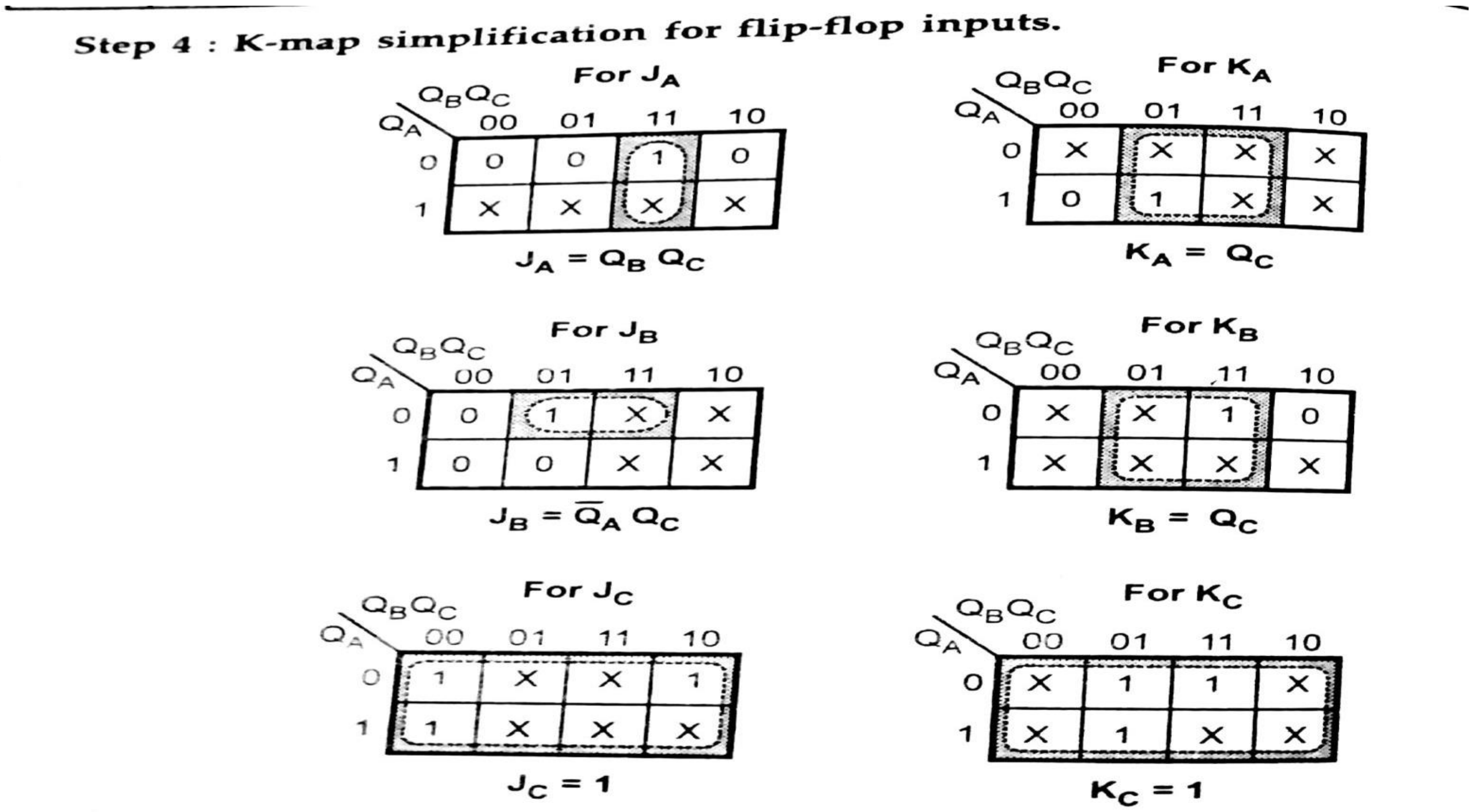
Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Design Synchronous MOD-6 Counter Using JK flip flop

Step 3 : Determine the transition table.

Present state			Next state			Flip-flop inputs					
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	x	0	x	1	x
0	0	1	0	1	0	0	x	1	x	x	1
0	1	0	0	1	1	0	x	x	0	1	x
0	1	1	1	0	0	1	x	x	1	x	1
1	0	0	1	0	1	x	0	0	x	1	x
1	0	1	0	0	0	x	1	0	x	x	1
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

Design Synchronous MOD-6 Counter Using JK flip flop



Design Synchronous MOD-6 Counter Using JK flip flop

Step 5 : Implement the counter.

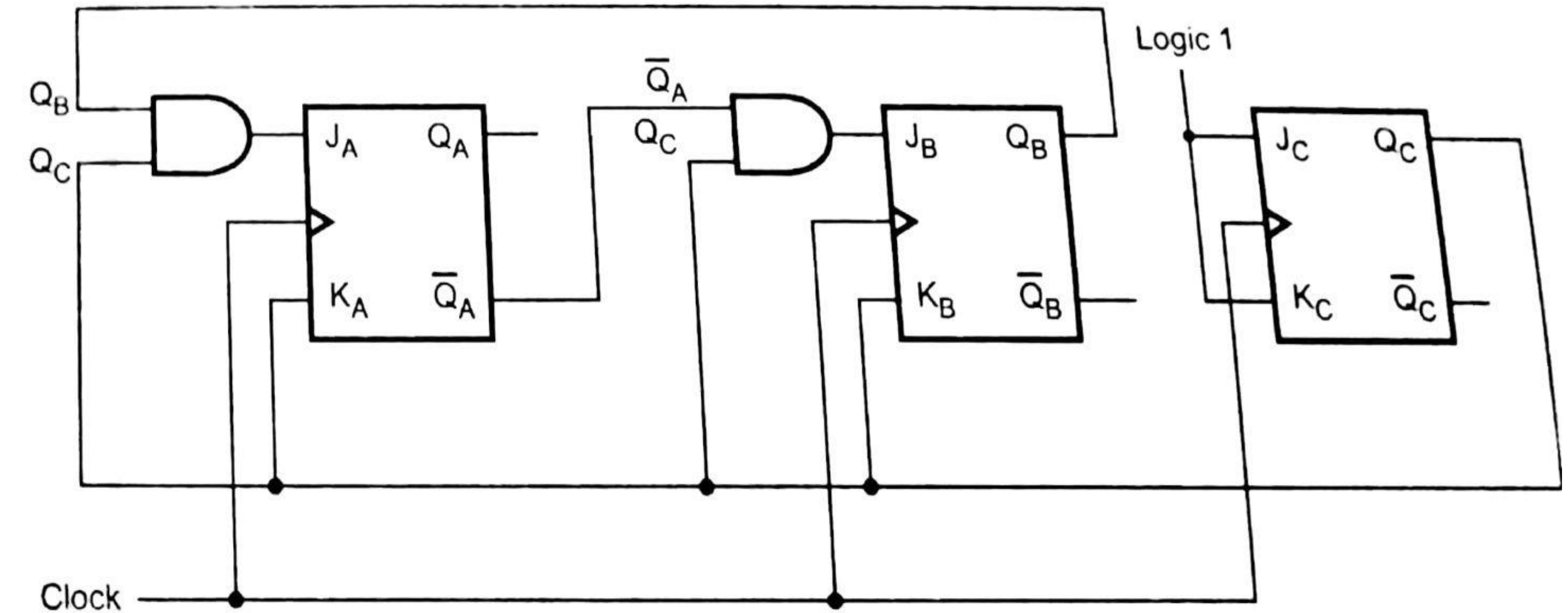


Fig. 7.79 Implementation of MOD 6 synchronous counter

Design Synchronous MOD-6 Counter Using D flip flop

Step 1 : Find number of flip-flops required to build the counter.

Flip-flops required are : $2^n \geq N$

Here $N = 6 \quad \therefore \quad n = 3$

i.e. Three flip-flops are required.

Design Synchronous MOD-6 Counter Using D flip flop

Step 2 : Determine the transition table.

Present state			Next state		
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	0	0	0
1	1	0	x	x	x
1	1	1	x	x	x

Design Synchronous MOD-6 Counter Using D flip flop

Step 3 : K-map simplification for flip-flop inputs.

For D_A

Q_A \ Q_BQ_C	00	01	11	10
0	0	0	1	0
1	1	0	X	X

$$D_A = Q_A\overline{Q_C} + Q_BQ_C$$

For D_B

Q_A \ Q_BQ_C	00	01	11	10
0	0	1	0	1
1	0	0	X	X

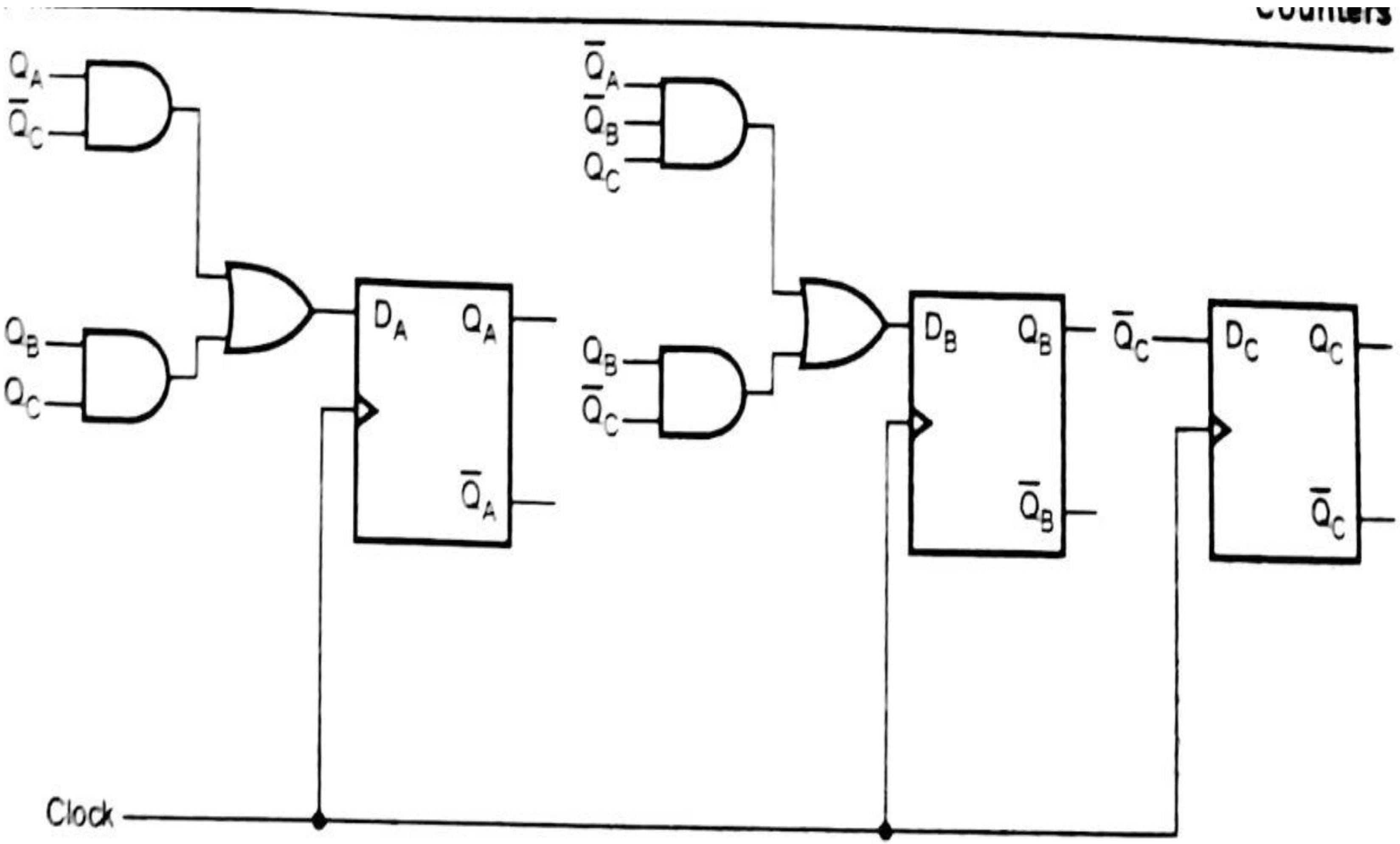
$$D_B = \overline{Q_A}\,\overline{Q_B}Q_C + Q_B\overline{Q_C}$$

For D_C

Q_A \ Q_BQ_C	00	01	11	10
0	1	0	0	1
1	1	0	X	X

$$D_C = \overline{Q_C}$$

Design Synchronous MOD-6 Counter Using D flip flop



Any Query????

Thank you……