SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

II YEAR / III SEMESTER

Unit III- **SEQUENTIAL CIRCUITS**

Topic : Design of Synchronous counter

Synchronous Sequential Circuit Models

Structural „

- •Logic diagram „
- • Excitation Equations „
- • Output equations

Behavioral „

- •Transition and output equations „
- •Transition table „
- • State table „
- • State diagram (graph)
- •¶SC Analysis: Derive one of the behavioral models from an instance of a structural model

¶SC Synthesis: Derive a structural model from one of the behavioral models

ANALYSIS OF SYNCHRONOUS SEQUENTIAL CIRCUITS

•The behavior of sequential circuit can be determined from the inputs, the output and state of its flip flops.

•The outputs and next state are both a function of its inputs and the present state.

•The analysis of a sequential circuit consists of obtaining a table or diagram for the time sequence of inputs, outputs and internal states.

Analysis Procedure

- Identify type of circuit either Mealy or Moore circuit
- Derive excitation equation (Boolean expression)
- Derive next state and output equations
- Generate state table
- Generate state diagram

Analysis Procedure

DESIGN PROCEDURE FOR CLOCKED SEQUENTIAL CIRCUIT

The following steps are followed to design the clocked sequential logic circuit.

•Obtain the state table from the given circuit information such as a state diagram, a timing diagram or description.

•The number of states may be reduced by state reduction technique.

•Assign binary values to each state in the state table.

•Determine the number of flip flops required and assign a letter symbol to each flip flop.

•Choose the flip flop type to be used according to the application.

•Derive the excitation table from the reduced state table.

•Derive the expression for flip flop inputs and outputs using k-map simplification (The present state and inputs are considered for k-map simplification) and draw logic circuit

Any Query????

Thank you……