SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

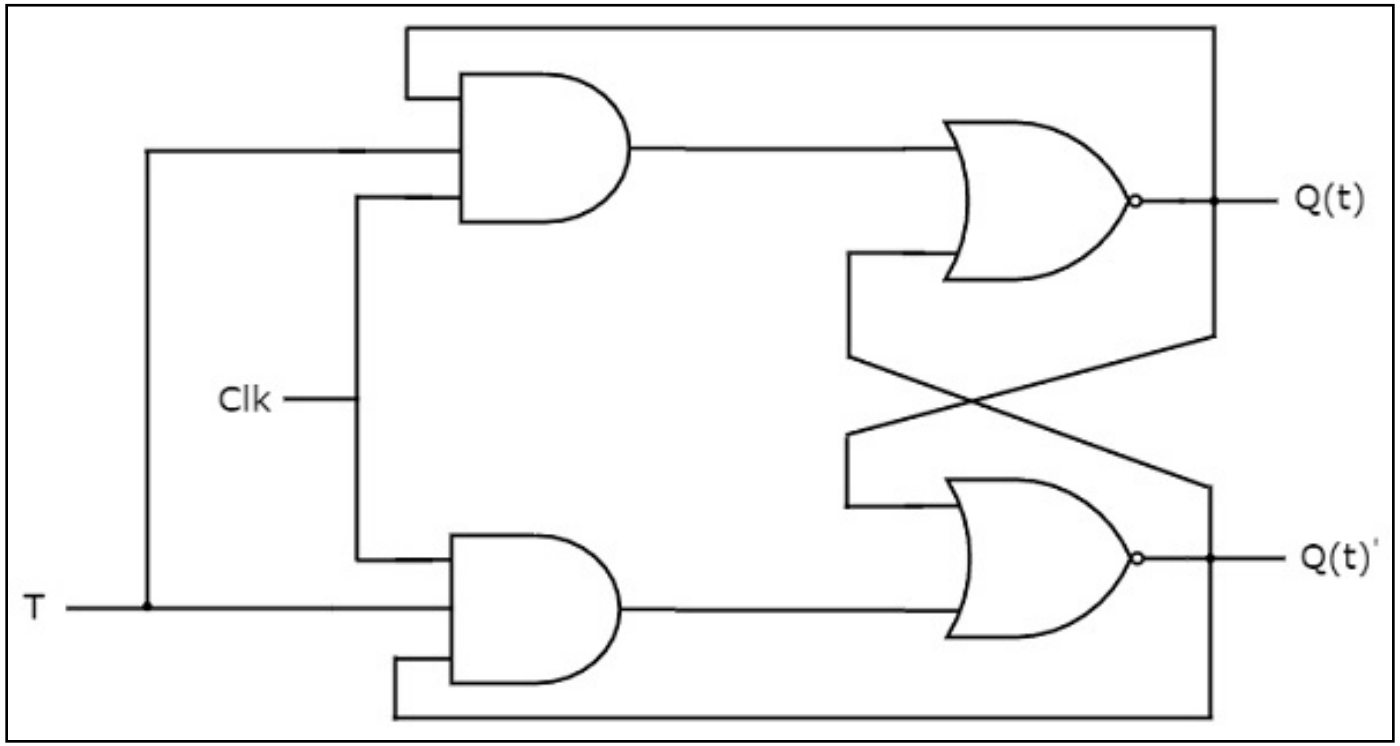
II YEAR / III SEMESTER

Unit III- **SEQUENTIAL CIRCUITS**

Topic : T,D and Master slave FF - Characteristic table and equation

T Flip-Flop

T flip-flop is the simplified version of JK flip-flop. It is obtained by connecting the same input 'T' to both inputs of JK flip-flop. It operates with only positive clock transitions or negative clock transitions.



T Flip-flop

Symbol

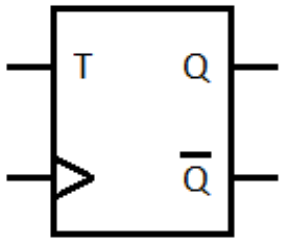


Table of truth:

T	Q	$\overline{Q}$
0	Q	$\overline{Q}$
1	$\overline{Q}$	Q
0	$\overline{Q}$	Q
1	Q	$\overline{Q}$

Inputs	Present State	Next State
T	Q t	Q $t+1$
0	0	0
0	1	1
1	0	1
1	1	0

$$Q(t+1) = T'Q(t) + TQ(t)'$$

$$\Rightarrow Q(t+1) = T \oplus Q(t)$$

T Flip-Flop- Characteristic Table & Equation

T flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Tables

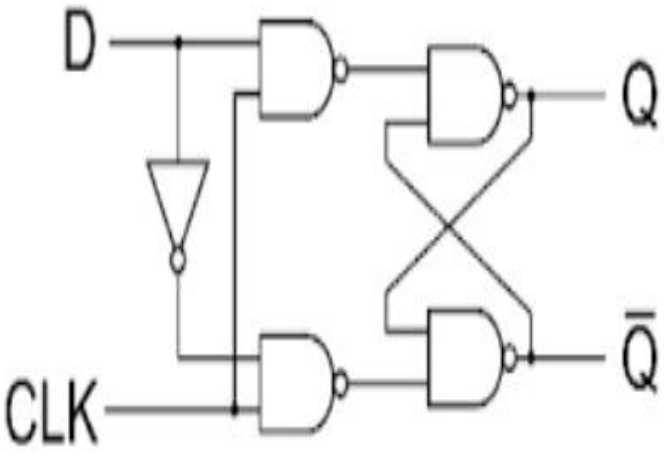
SR Flip-flop			
Q(t)	Q(t+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

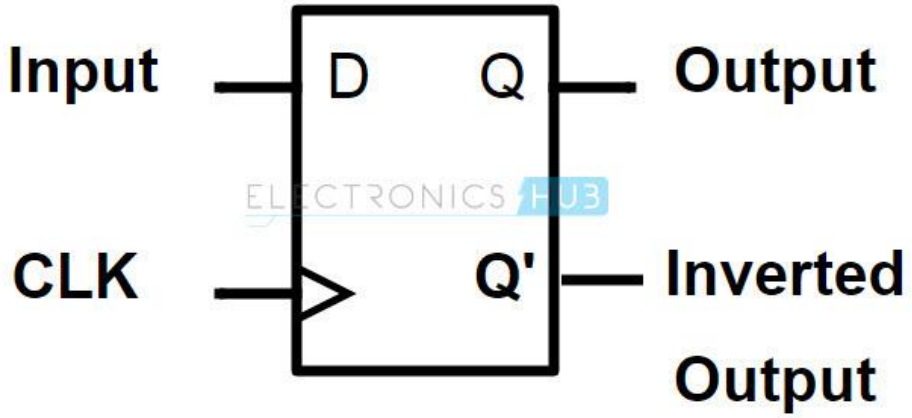
D Flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	0
1	1	1

JK flip-flop			
Q(t)	Q(t+1)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T flip-flop		
Q(t)	Q(t+1)	DR
0	0	0
0	1	1
1	0	1
1	1	0

D FLIP FLOP

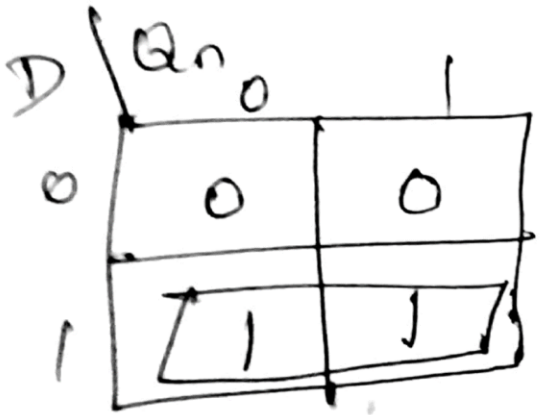




D FLIP FLOP –TRUTH TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1
0	0	0
0	1	1
1	0	1
1	1	1

Characteristic Equation



$$Q_{n+1} = D$$

Excitation table

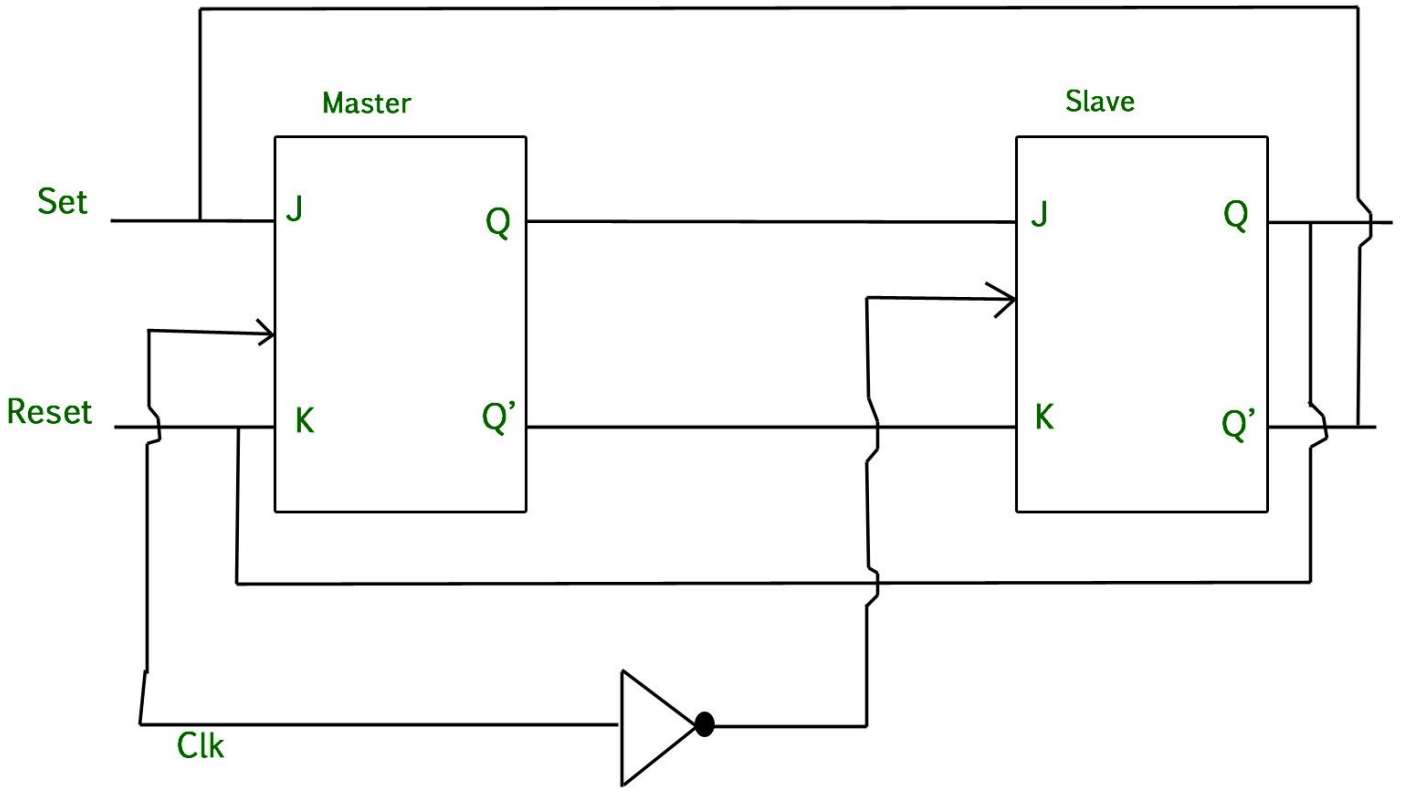
Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Master-Slave JK Flip Flop

The Master-Slave Flip-Flop is basically a combination of two JK flip-flops connected together in a series configuration. Out of these, one acts as the **“master”** and the other as a **“slave”**.

The output from the master flip flop is connected to the two inputs of the slave flip flop whose output is fed back to inputs of the master flip flop. In addition to these two flip-flops, the circuit also includes an **inverter**. The inverter is connected to clock pulse in such a way that the inverted clock pulse is given to the slave flip-flop.

In other words if CP=0 for a master flip-flop, then CP=1 for a slave flip-flop and if CP=1 for master flip flop then it becomes 0 for slave flip flop.



Master-slave JK Flip-Flop

Working of a master slave flip flop –

1.When the clock pulse goes to 1, the slave is isolated; J and K inputs may affect the state of the system. The slave flip-flop is isolated until the CP goes to 0. When the CP goes back to 0, information is passed from the master flip-flop to the slave and output is obtained.

2.Firstly the master flip flop is positive level triggered and the slave flip flop is negative level triggered, so the master responds before the slave.

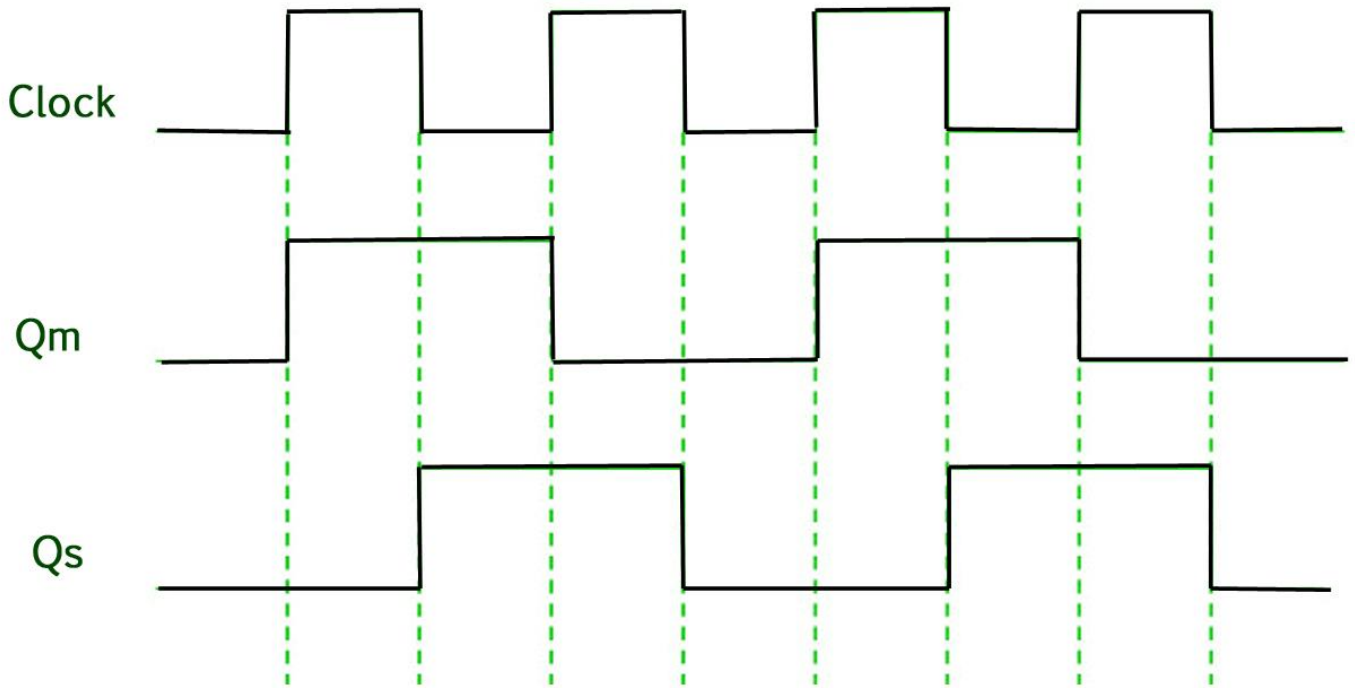
3.If J=0 and K=1, the high Q' output of the master goes to the K input of the slave and the clock forces the slave to reset, thus the slave copies the master.

4.If J=1 and K=0, the high Q output of the master goes to the J input of the slave and the Negative transition of the clock sets the slave, copying the master.

5.If J=1 and K=1, it toggles on the positive transition of the clock and thus the slave toggles on the negative transition of the clock.

6.If J=0 and K=0, the flip flop is disabled and Q remains unchanged.

Timing Diagram of a Master Slave flip flop



1.When the Clock pulse is high the output of master is high and remains high till the clock is low because the state is stored.

2.Now the output of master becomes low when the clock pulse becomes high again and remains low until the clock becomes high again.

3.Thus toggling takes place for a clock cycle.

4.When the clock pulse is high, the master is operational but not the slave thus the output of the slave remains low till the clock remains high.

5.When the clock is low, the slave becomes operational and remains high until the clock again becomes low.

6.Toggling takes place during the whole process since the output is changing once in a cycle.

Any Query????

Thank you……