SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

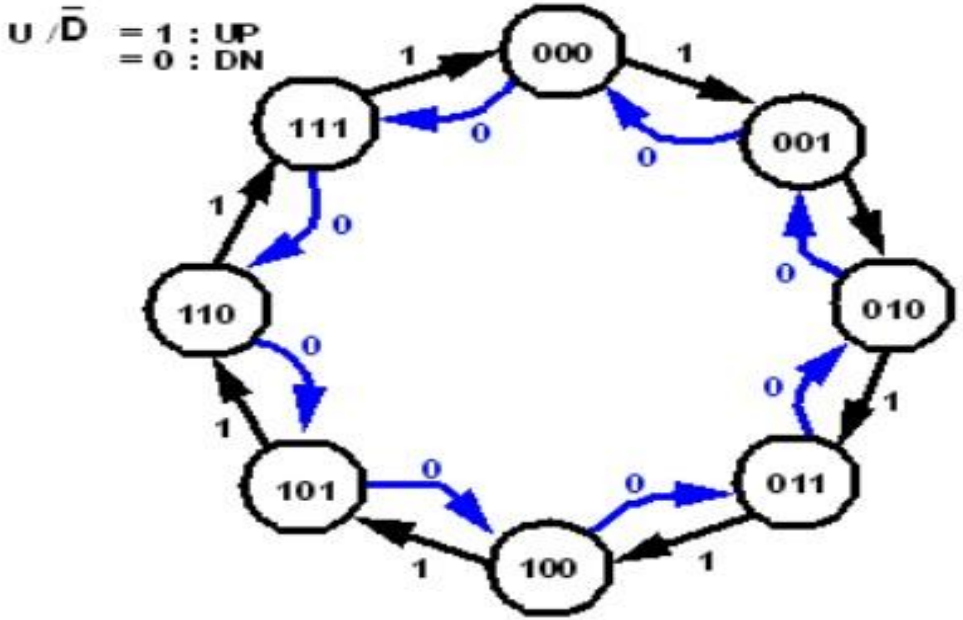
II YEAR / III SEMESTER

Unit III- Sequential circuits
Topic : Up/ Down Counter

3-bit Synchronous Up/Down Counter

Up/Down Counters

- A 3-bit binary up/down counter (State diagram)



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3-bit Synchronous Down Counter

State Table

CP	UP	Q_C	Q_B	Q_A	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

3-bit Synchronous Down Counter

Excitation table

Input	Present State			Next State			Flip-flop Inputs		
UP/DOWN (UD)	Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	1
0	0	1	0	0	0	1	0	1	1
0	0	1	1	0	1	0	0	0	1
0	1	0	0	0	1	1	1	1	1
0	1	0	1	1	0	0	0	0	1
0	1	1	0	1	0	1	0	1	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	1	0	0	1
1	0	0	1	0	1	0	0	1	1
1	0	1	0	0	1	1	0	0	1
1	0	1	1	1	0	0	1	1	1
1	1	0	0	1	0	1	0	0	1
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	0	0	1
1	1	1	1	0	0	0	1	1	1

3-bit Synchronous Down Counter

K-map simplification

For T_C

UD Q_C \ Q_BQ_A	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	0	0	1	0
10	0	0	1	0

$T_C = \overline{UD}\ \overline{Q}_B\ \overline{Q}_A + UD\ Q_B\ Q_A$

For T_B

UD Q_C \ Q_BQ_A	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	0	1	1	0
10	0	1	1	0

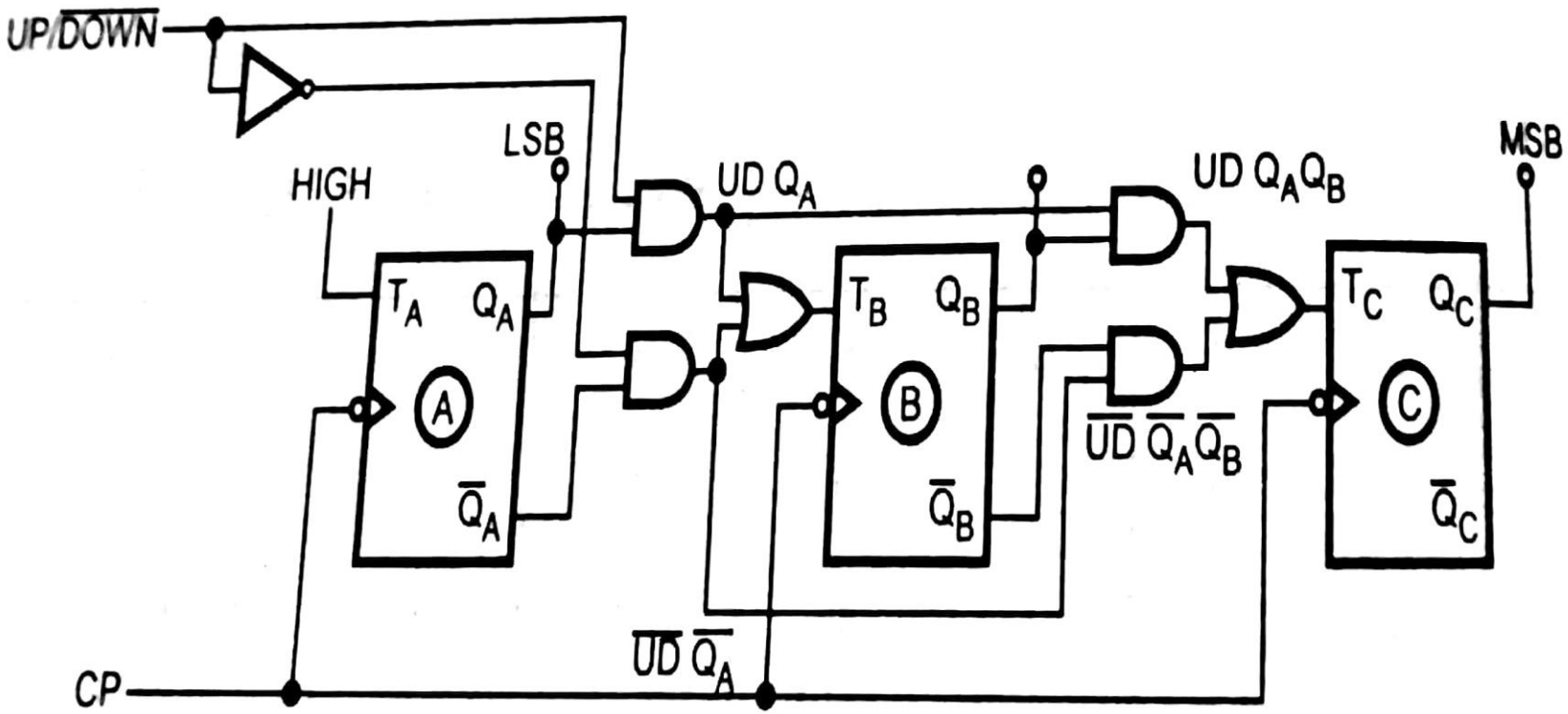
$T_B = \overline{UD}\ \overline{Q}_A + UD\ Q_A$

For T_A

UD Q_C \ Q_BQ_A	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$T_A = 1$

Logic Diagram



Any Query????

Thank you……