SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

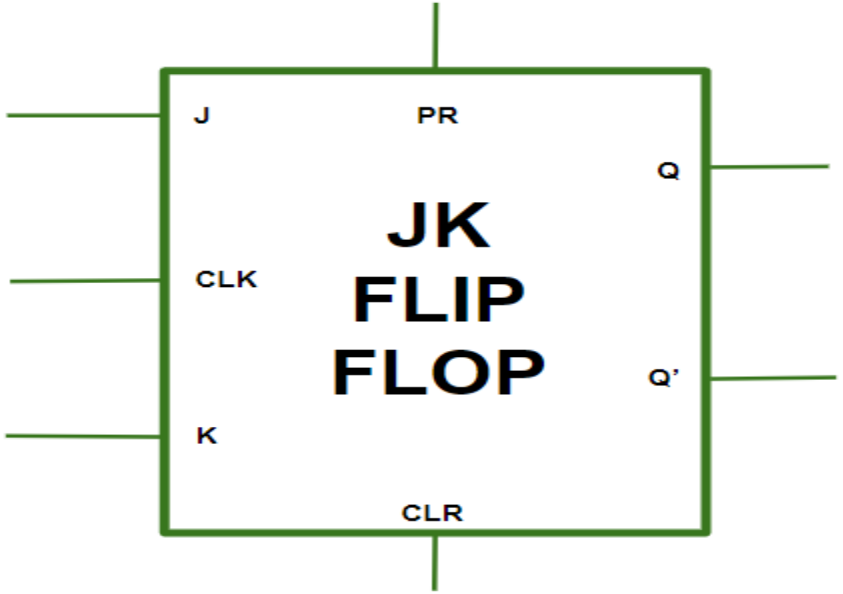
II YEAR / III SEMESTER

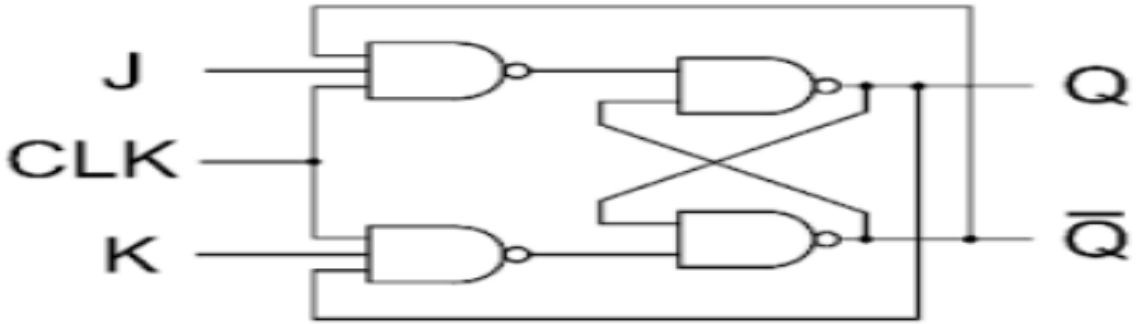
Unit III- **Sequential circuits**

Topic : JK FF - Characteristic table and equation

J-K Flip Flop:

In JK flip flops, the diagram over here represents the basic structure of the flip flop which consists of Clock (CLK), Clear (CLR), Preset (PR).





TRUTH TABLE

J	K	Q_N	Q_{N+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Operations:

Case 1:
PR=CLR=0 This condition is in its invalid state.

Case 2:
PR=0 and CLR=1 The PR is activated which means the output in the Q is set to 1. Therefore, the flip flop is in the set state.

Case 3:
PR=1 and CLR=0 The CLR is activated which means the output in the Q' is set to 1. Therefore, the flip flop is in the reset state.

Case 4:

PR=CLR=1 In this condition the flip flop works in its normal way whereas the PR and CLR gets deactivated.

Race around condition:

When the J and K both are set to 1, the input remains high for a longer duration of time, then the output keeps on toggling. Toggle means that switching in the output instantly i.e. Q=0, Q'=1 will immediately change to Q=1 and Q'=0 and this continuation keeps on changing. This change in output leads to race around condition.

Characteristics Equation for JK Flip Flop: $Q_{N+1} = JQ'_N + K'Q_N$

Any Query????

Thank you……