



SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

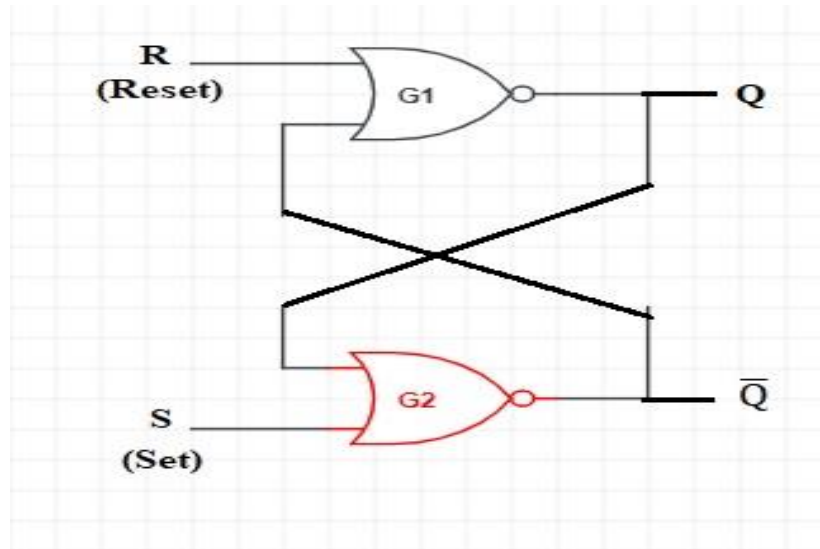
II YEAR / III SEMESTER

Unit III- Sequential circuits

**Topic : Latches, DT application edge triggering FF SR
characteristics table and equation**

SR Latch using NOR gates:

Latch is basic storage element in which we store 0 or 1. Latch as name suggest it holds 0 or 1. In the circuit “R” stands for reset and “S” stand for set. Q and \bar{Q} are the output of the latch. When the circuit will be reset Q value will be equal to 0 and when the circuit will be set the Q value will be equal to 1.





Case 1:

When the $S = 0$ and $R = 1$ and we will study the Q and \bar{Q} output
As we are using NOR gate and its truth table is:

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Case 2:

When $S = 1$, $R = 0$ then we will see that what will be the values of Q and \bar{Q} output:



Case 3:

When $S = 1$, $R = 1$ then we will see that what will be the values of Q and Q' output:

S	R	Q	Q'
0	0	Previous state	
0	1	0	1
1	0	1	0
1	1	Not used	



SR Flip Flop truth table:

Clk	S	R	Q	Q ⁻
0	x	x	Previous state	
1	0	0	Previous state	
1	0	1	0	1
1	1	0	1	0
1	1	1	Invalid	

Characteristics equation for SR flip flop:

Clk	S	R	Q _{n+1}
0	x	x	
1	0	0	
1	0	1	0 reset
1	1	0	1 set
1	1	1	Invalid



By using this table we will draw its characteristics table:

Q_n	S_n	R_n	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	×
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	×



Any Query????

Thank you.....