SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : 19EC306 – Digital Circuits

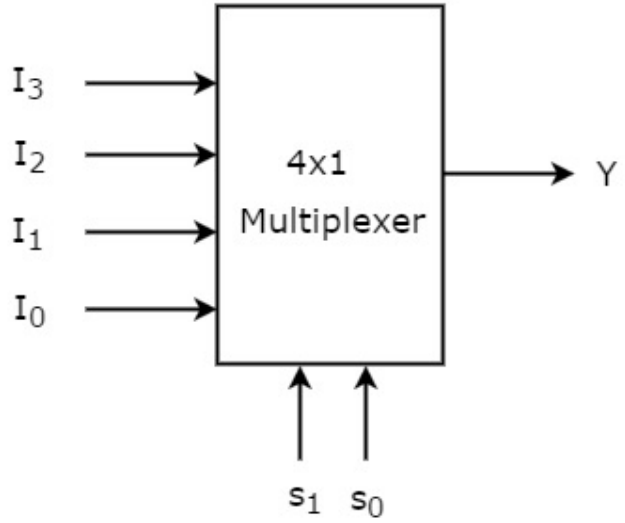
II YEAR / III SEMESTER

Unit I- **COMBINATIONAL CIRCUITS**

Topic : Binary multiplier, MUX and DEMUX

Multiplexer

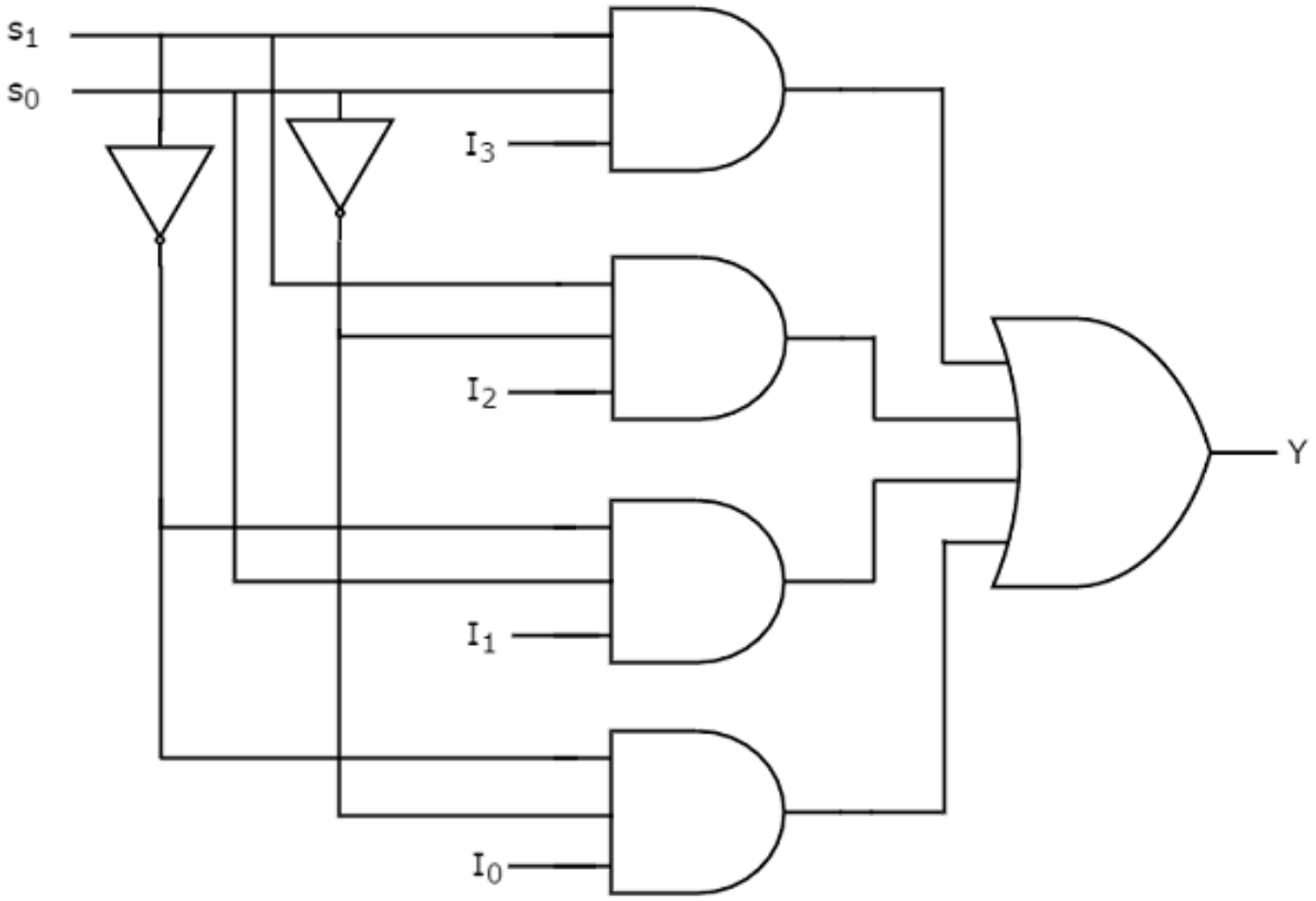
- Multiplexer is a combinational circuit that has maximum of 2n data inputs, ‘n’ selection lines and single output line.
- One of these data inputs will be connected to the output based on the values of selection lines..



- 4x1 Multiplexer has four data inputs I3, I2, I1 & I0, two selection lines s1 & s0 and one output Y.

- One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines.

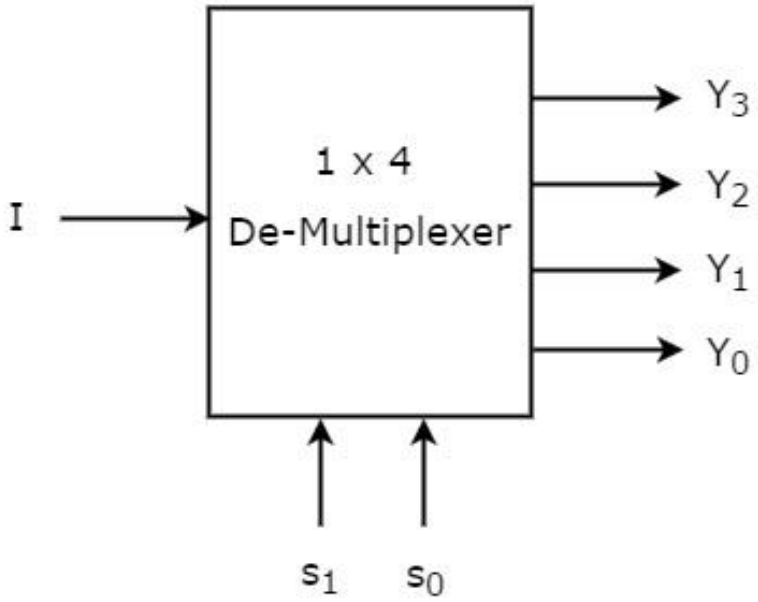
Selection Lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3


S1
S0
I3
I2
I1
I0
Y

De Multiplexer

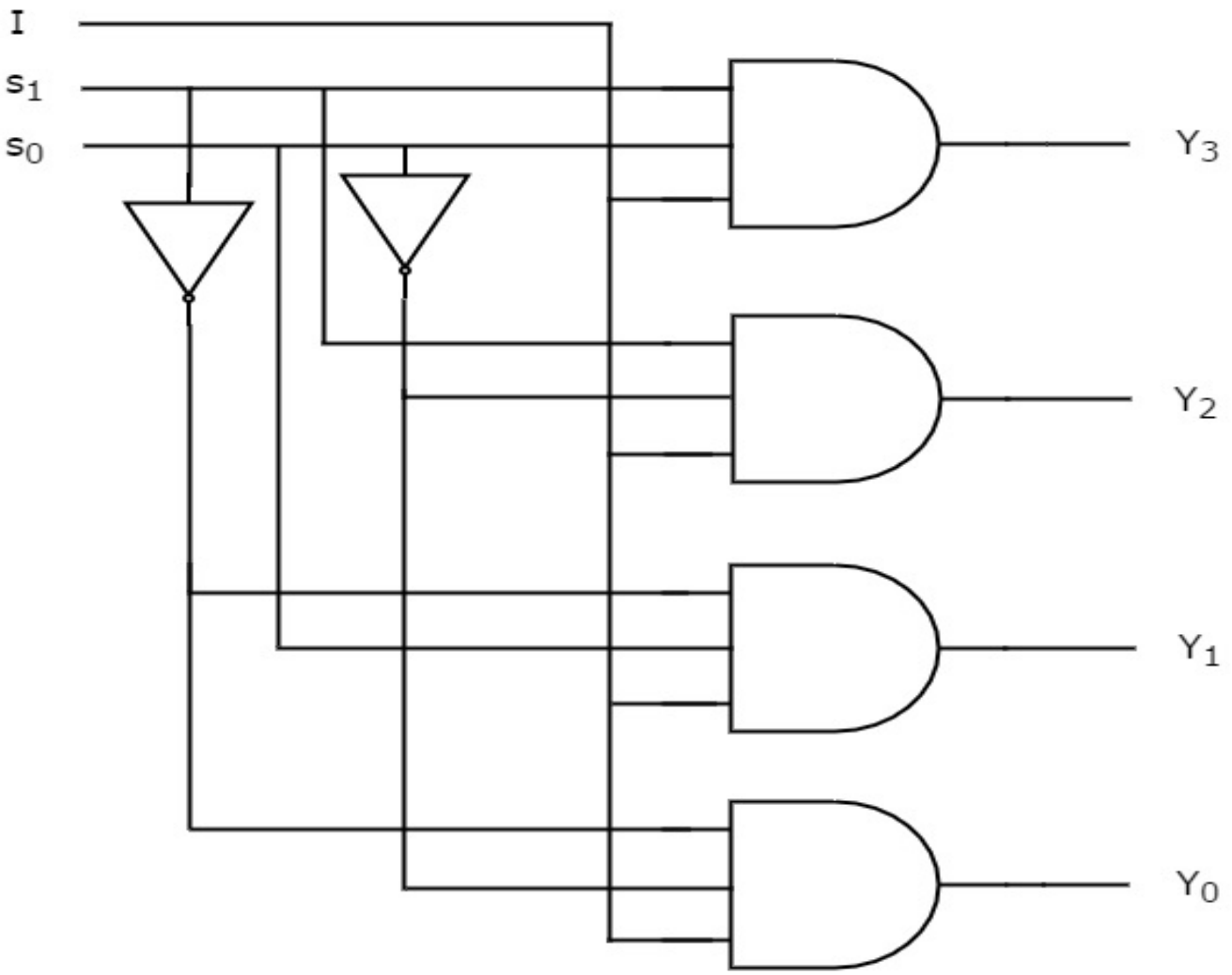
- De-Multiplexer is a combinational circuit that performs the reverse operation of Multiplexer. It has single input, ‘n’ selection lines and maximum of 2n outputs.

- One of these data inputs will be connected to the output based on the values of selection lines..



Selection Inputs		Outputs			
S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

- The single input 'I' will be connected to one of the four outputs, Y3 to Y0 based on the values of selection lines s1 & s0. The Truth table of 1x4 De-Multiplexer is shown below.

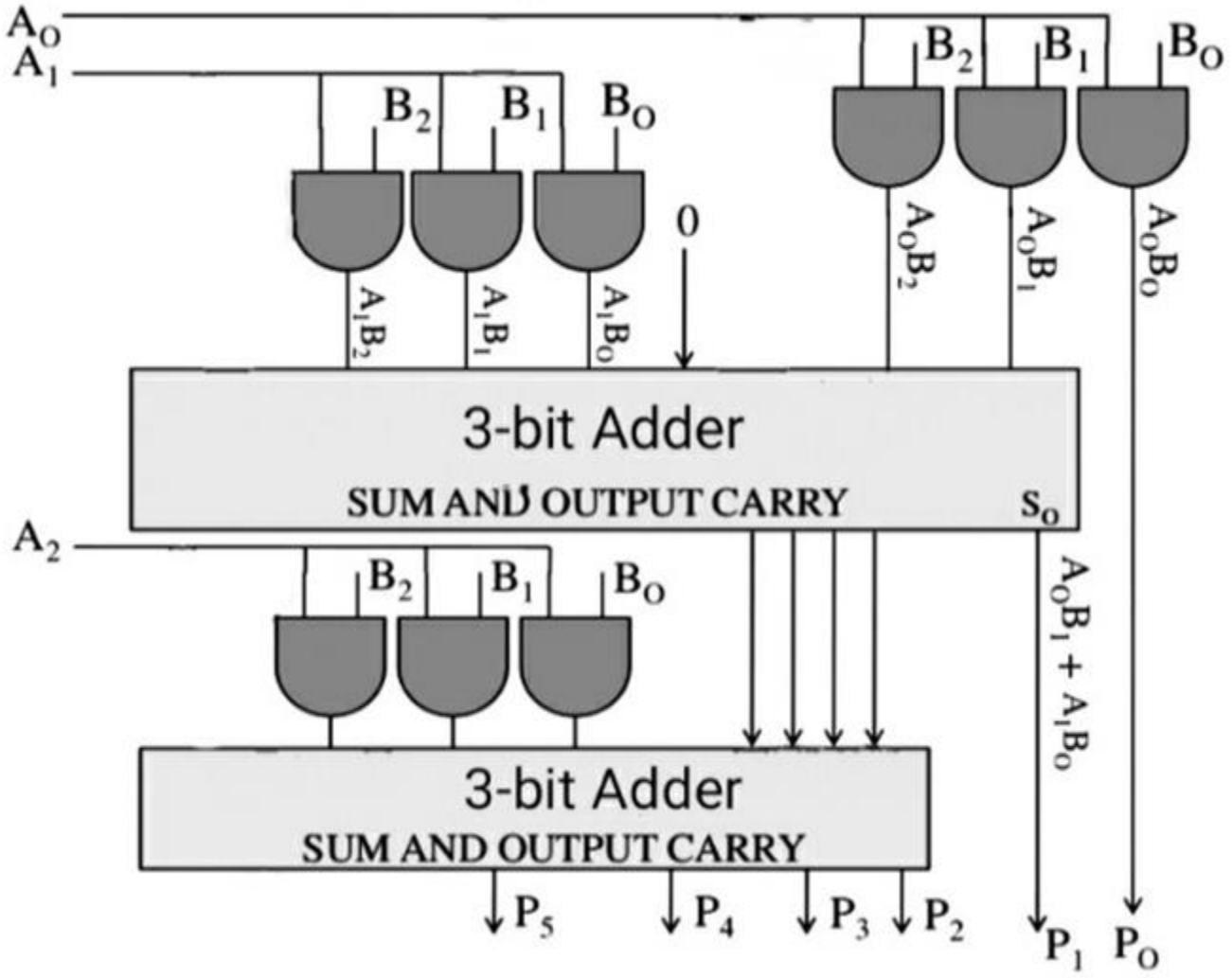

I
s_1
s_0
Y_3
Y_2
Y_1
Y_0

Binary multiplier:

A binary multiplier is used to multiply two binary numbers. It is a basic electronic circuit in digital electronics, such as a computer. The binary multiplier is also called an **add-shift adder.**

A digital multiplier can be implemented using a variety of computer arithmetic techniques. The majority of techniques involve computing a set of partial products, which are then summed using binary adders.

A2 A1 A0 (multiplicand)
X B2 B1 B0 (multiplier)
————————————————
A2B0 A1B0 A0B0
A2B1 A1B1 A0B1 XX
A2B2 A1B2 A0B2 X X
————————————————————
A2B2+C+C A2B2+A1B2+A2B2+C+C A1B1+C+A0B2+A2B0 A0B1+A1B0 A0B


A0
A1
B2
B1
B0
0
A0B2
A0B1
A0B0
A1B2
A1B1
A1B0
3-bit Adder
SUM AND OUTPUT CARRY
S0
A2
B2
B1
B0
A0B1 + A1B0
3-bit Adder
SUM AND OUTPUT CARRY
P5
P4
P3
P2
P1
P0

Any Query????

Thank you……