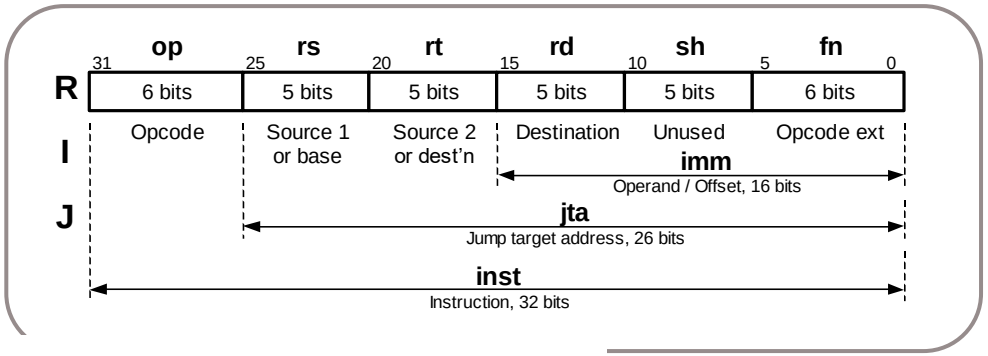
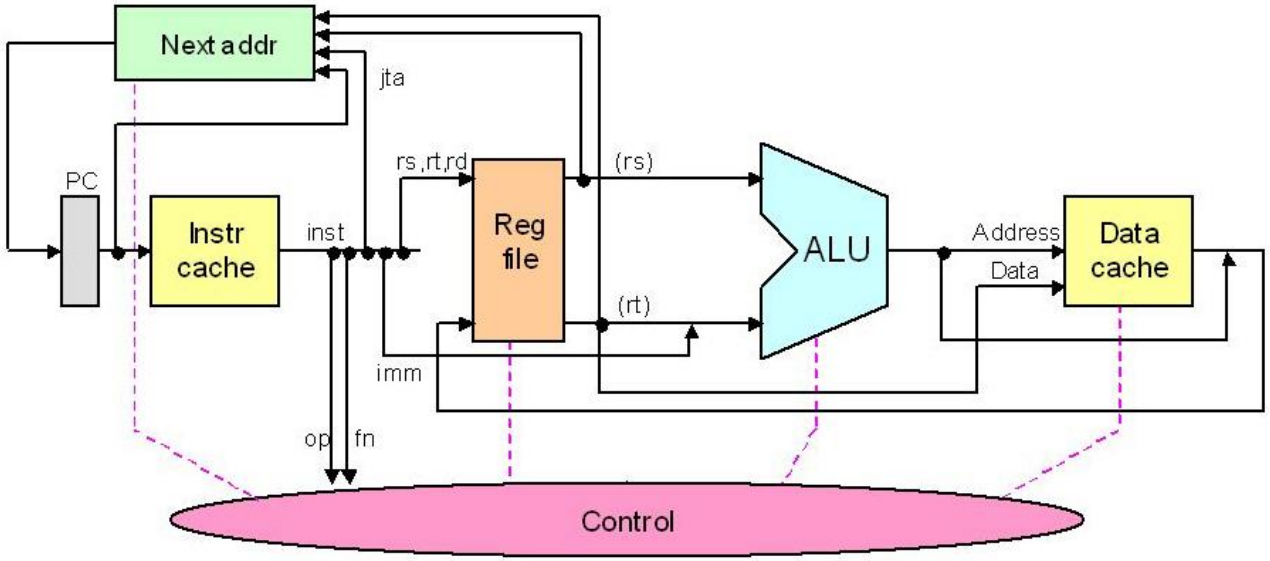
UNIT III
PROCESSOR AND CONTROL UNIT

Basic MIPS implementation – **Building datapath** – Control Implementation scheme – Pipelining – Pipelined datapath and control – Handling Data hazards & Control hazards – Exceptions.

Building Datapath

Recall the Prior Knowledge





Introduction

Major components is required to execute each class in **MIPS Instruction**

Components required for data path is called **Data path Element**

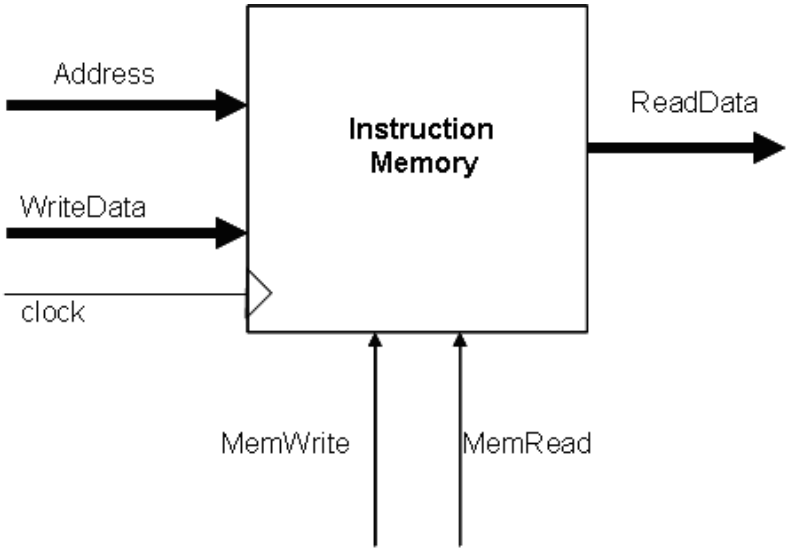
Data path: Elements that **process data and addresses in the CPU (on or hold data within the Processor)**

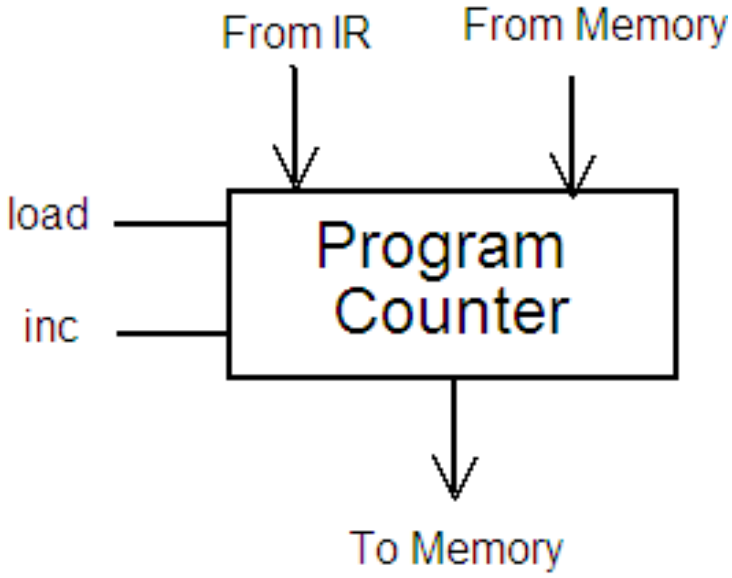
- Instruction and data memories, Registers, ALUs, and Adders

Introduction

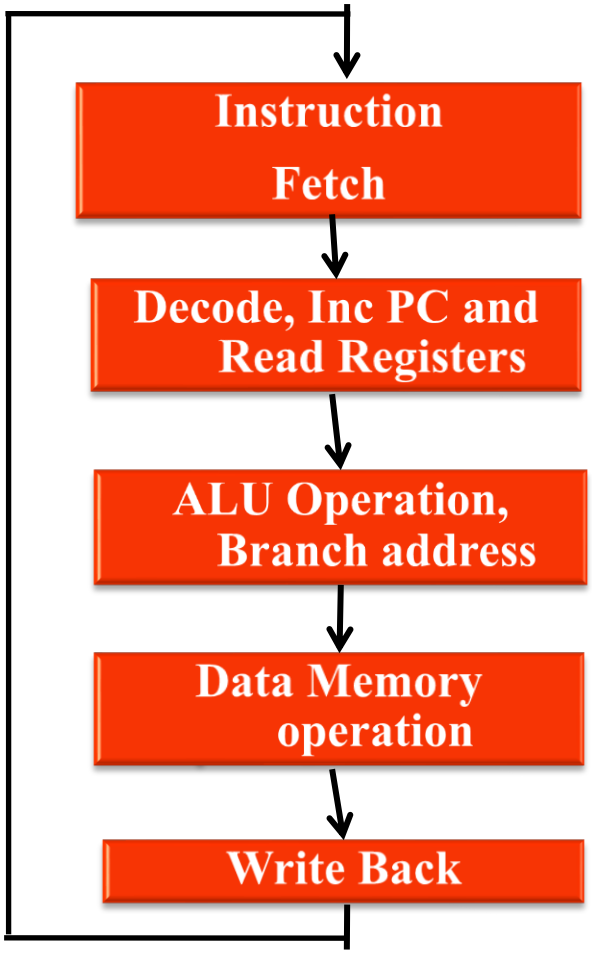
- the arithmetic-logical instructions add, sub, and, or and slt
- the memory-reference instructions lw and sw
- the flow-of-control instructions beq and j

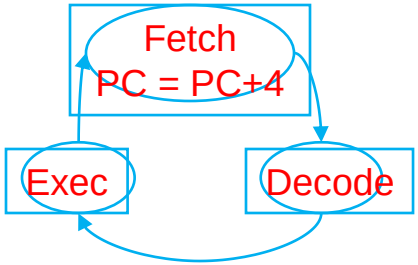
Introduction



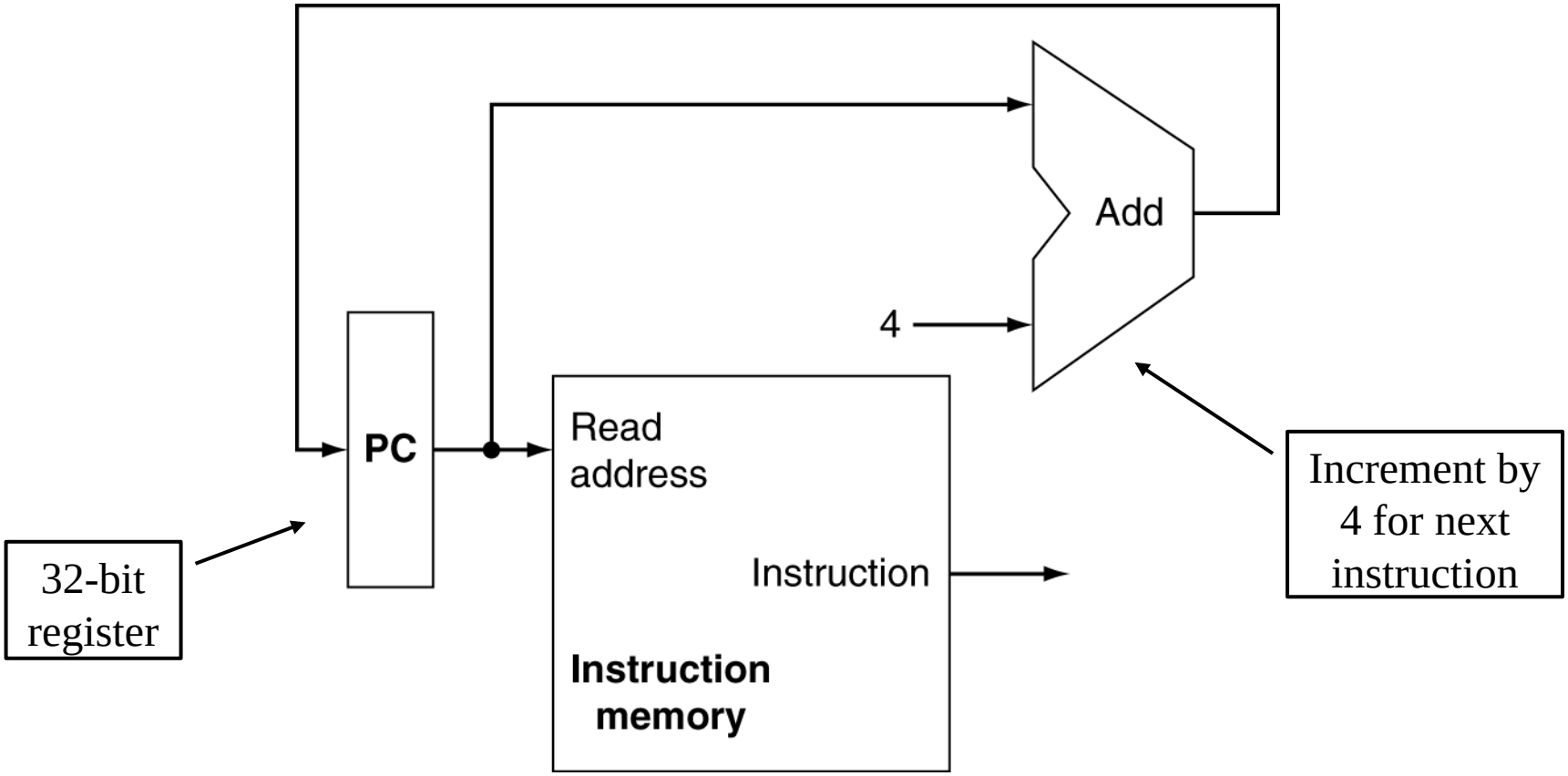


Instruction Execution Steps

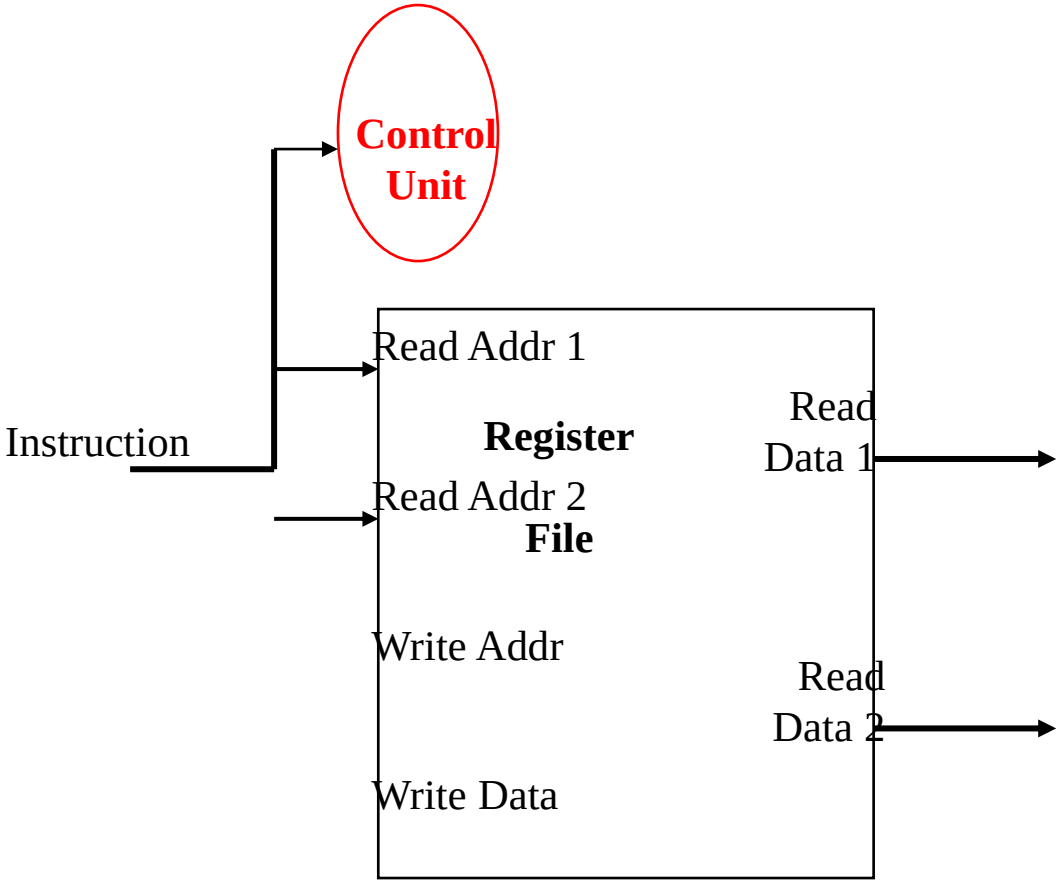




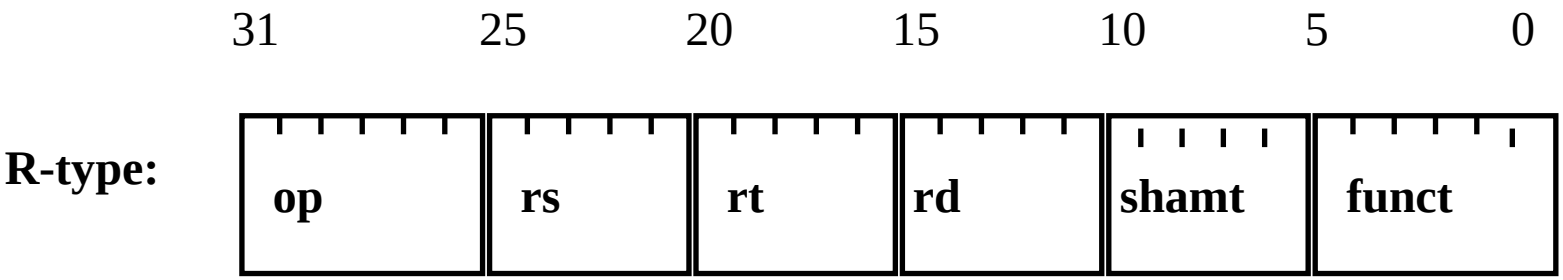
Fetching Instructions

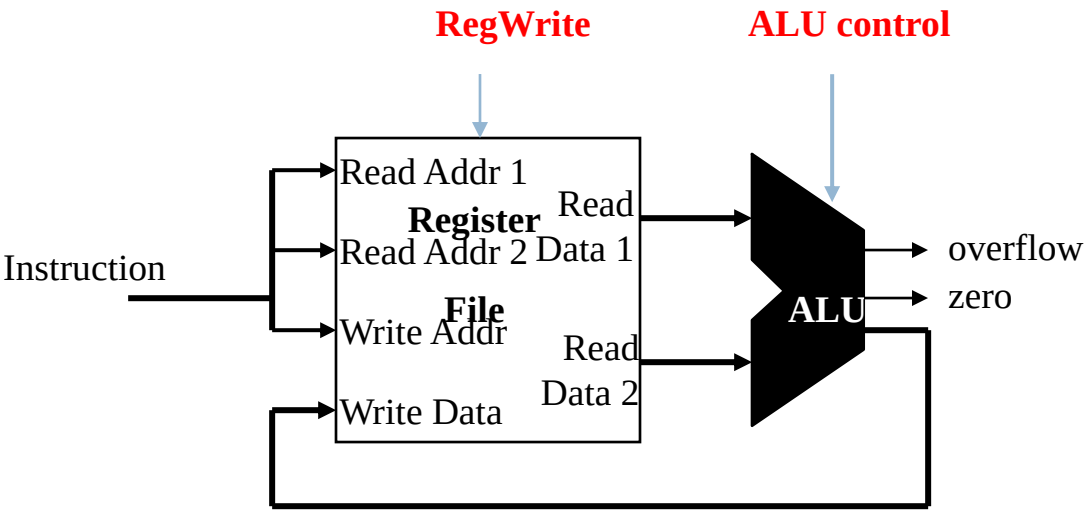


Decoding Instructions

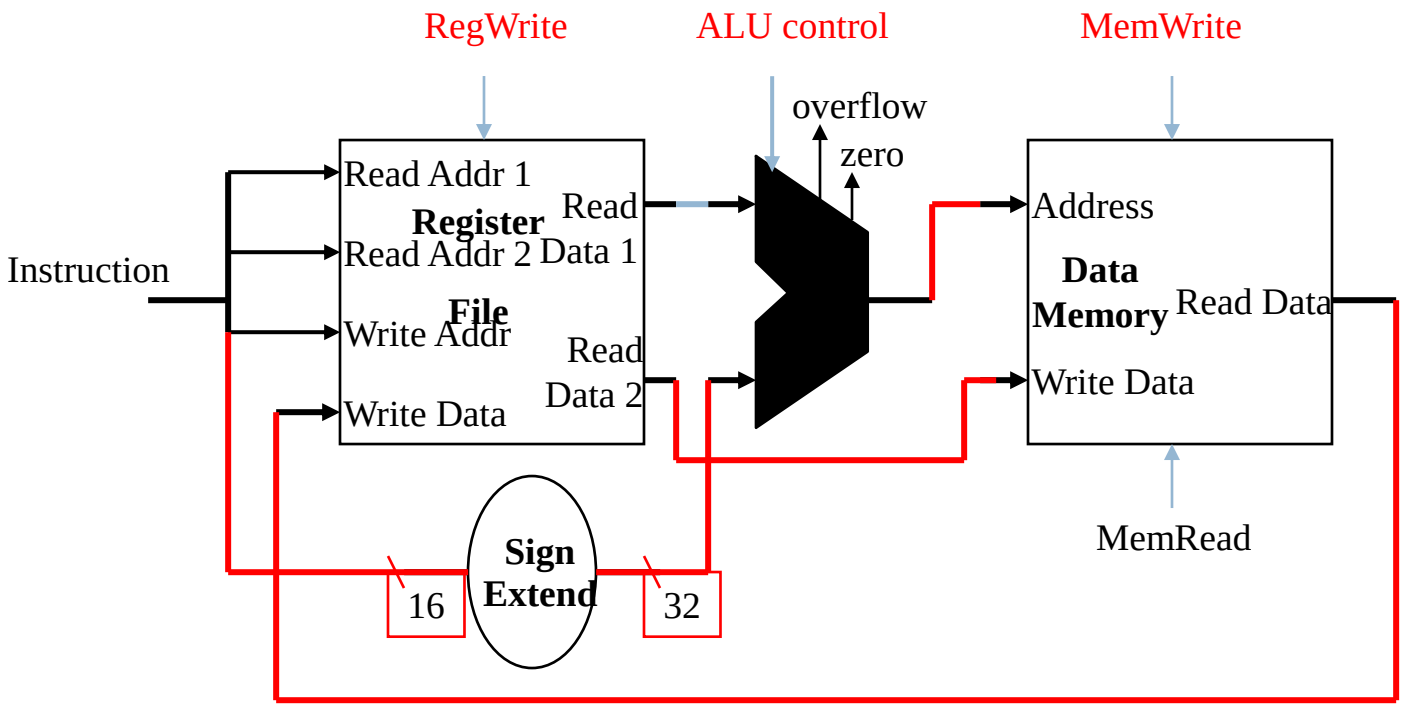


Executing R Format Operations

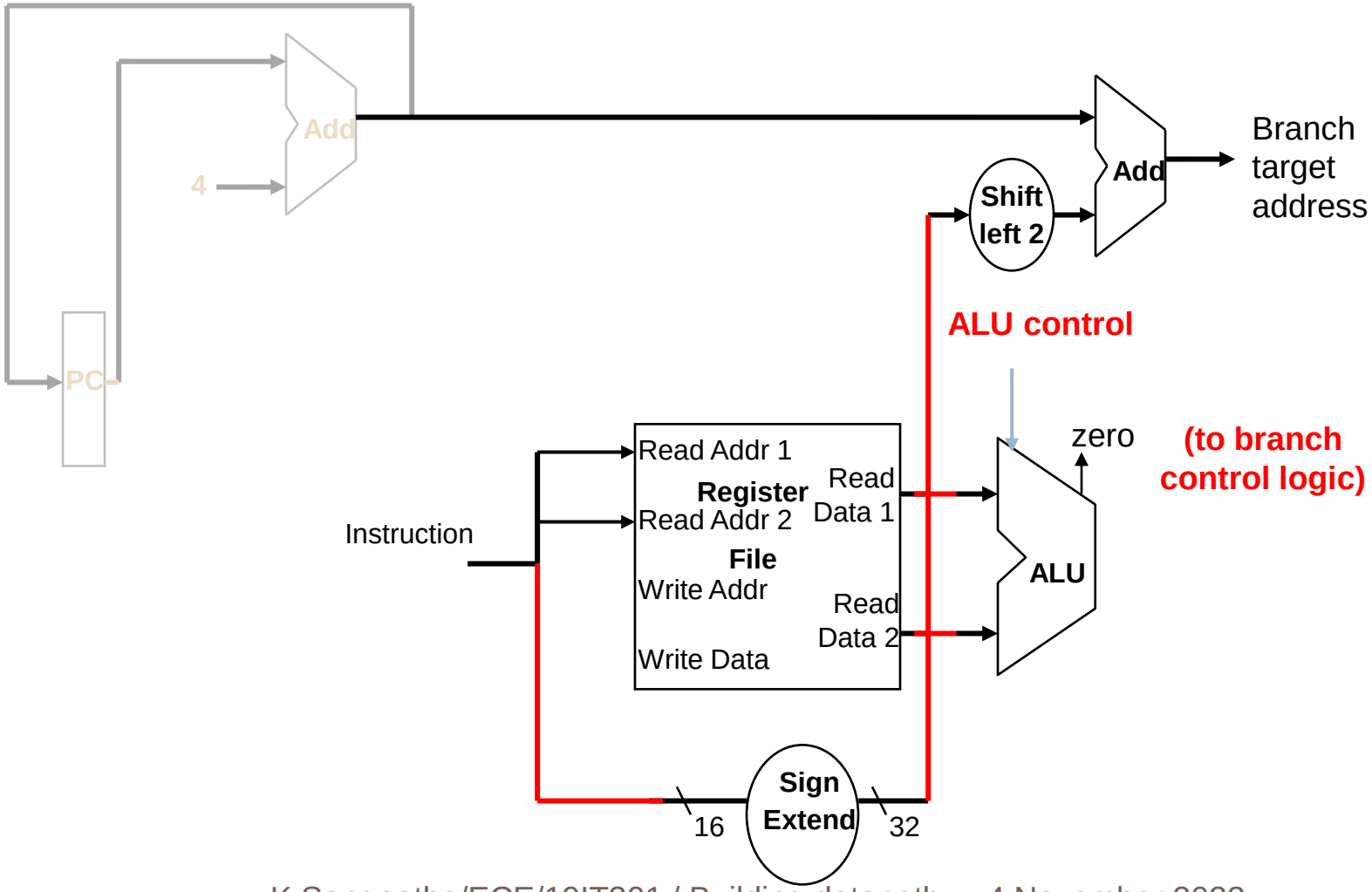




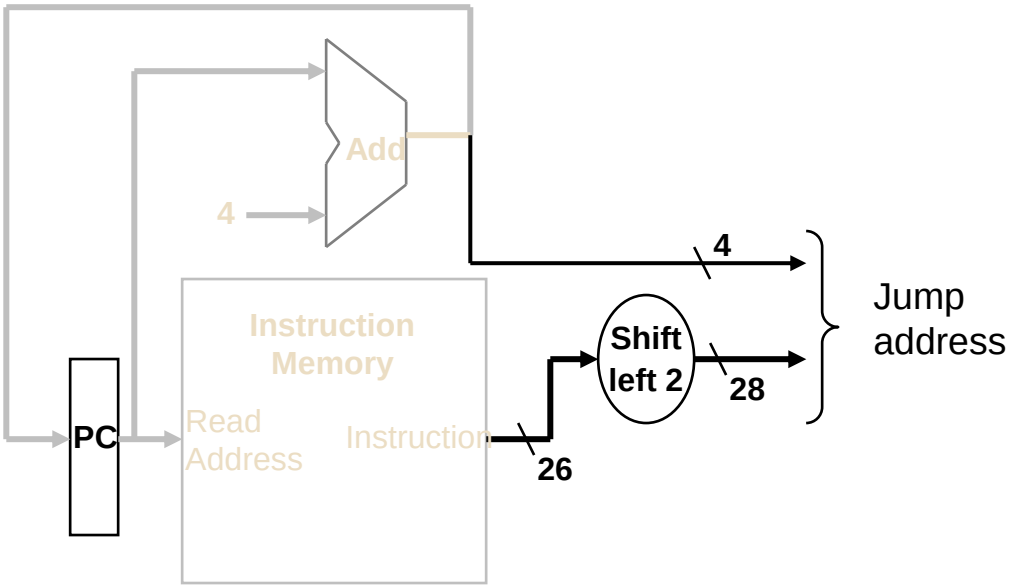
Executing Load and Store Operations



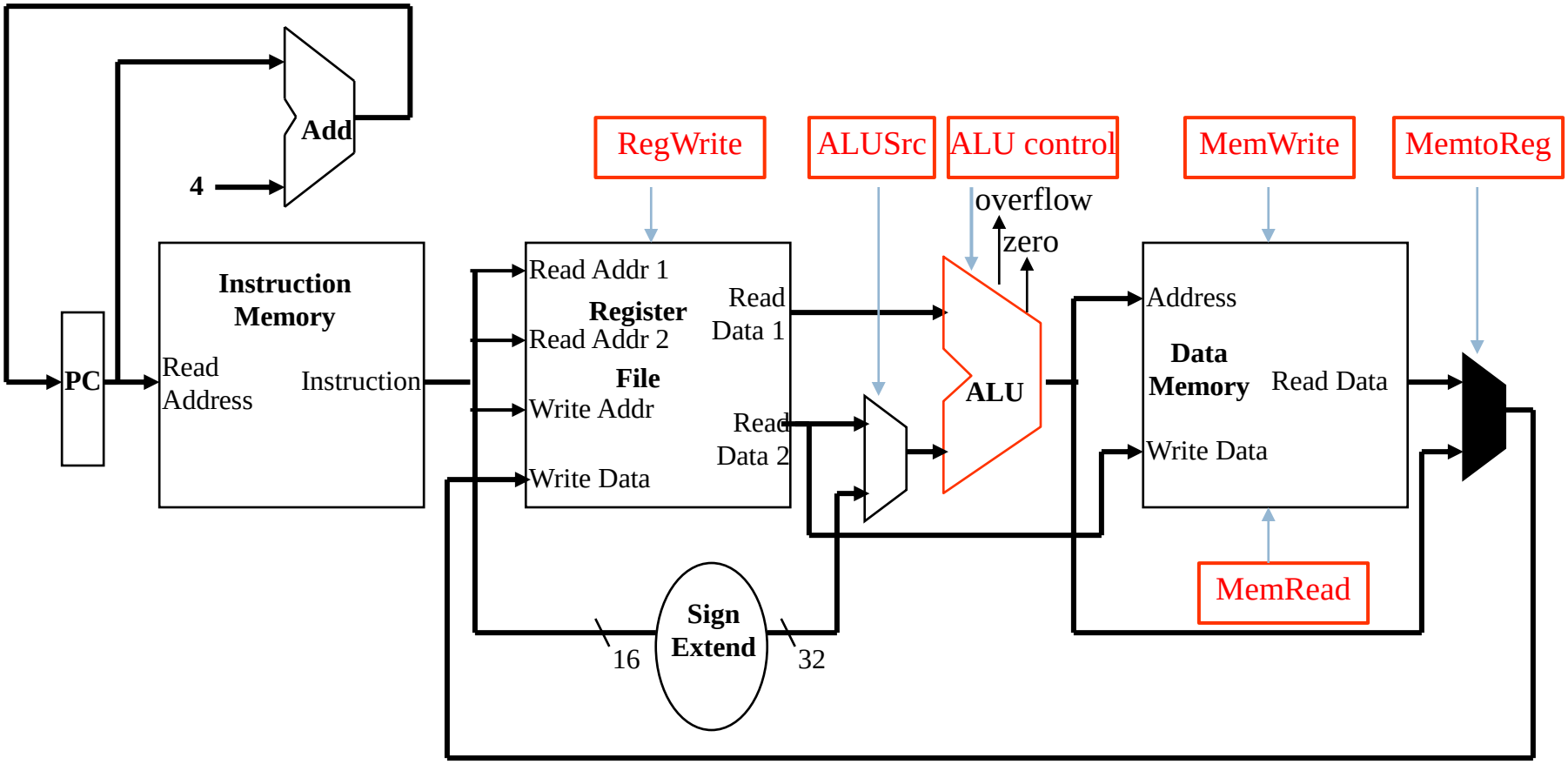
Executing Branch Operations



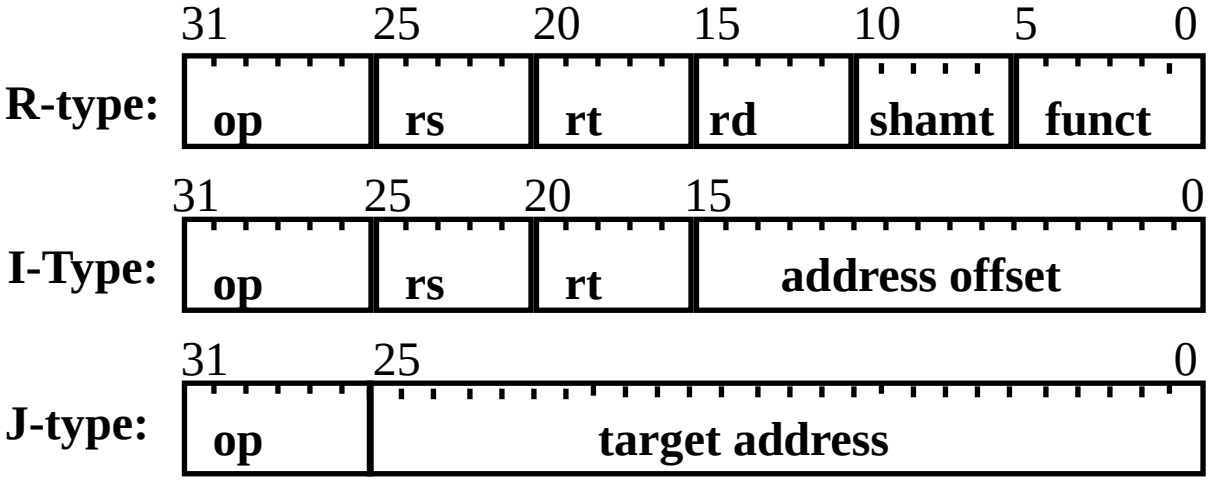
Executing Jump Operations



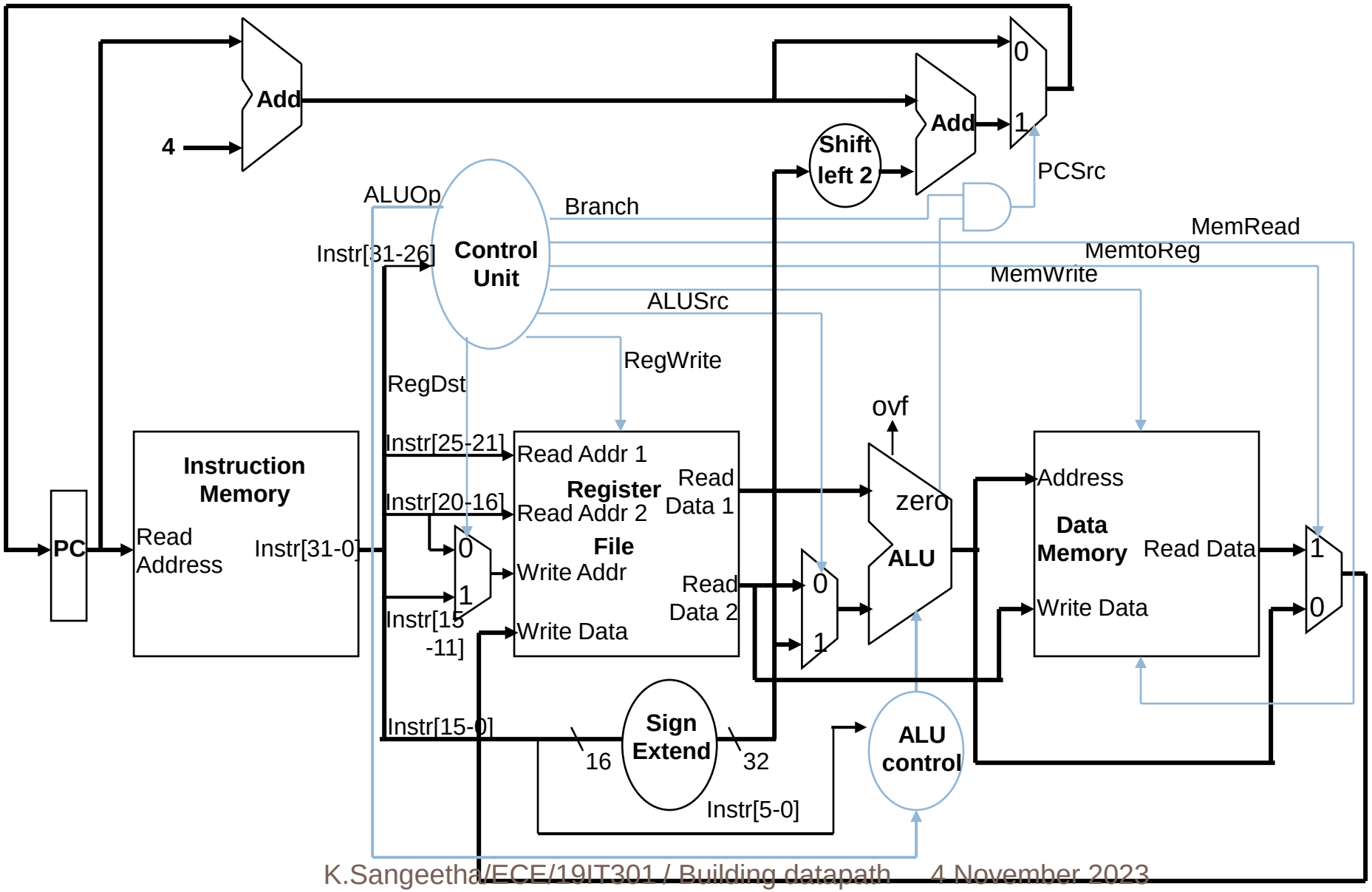
Fetch, R-type, and Memory Access Portions



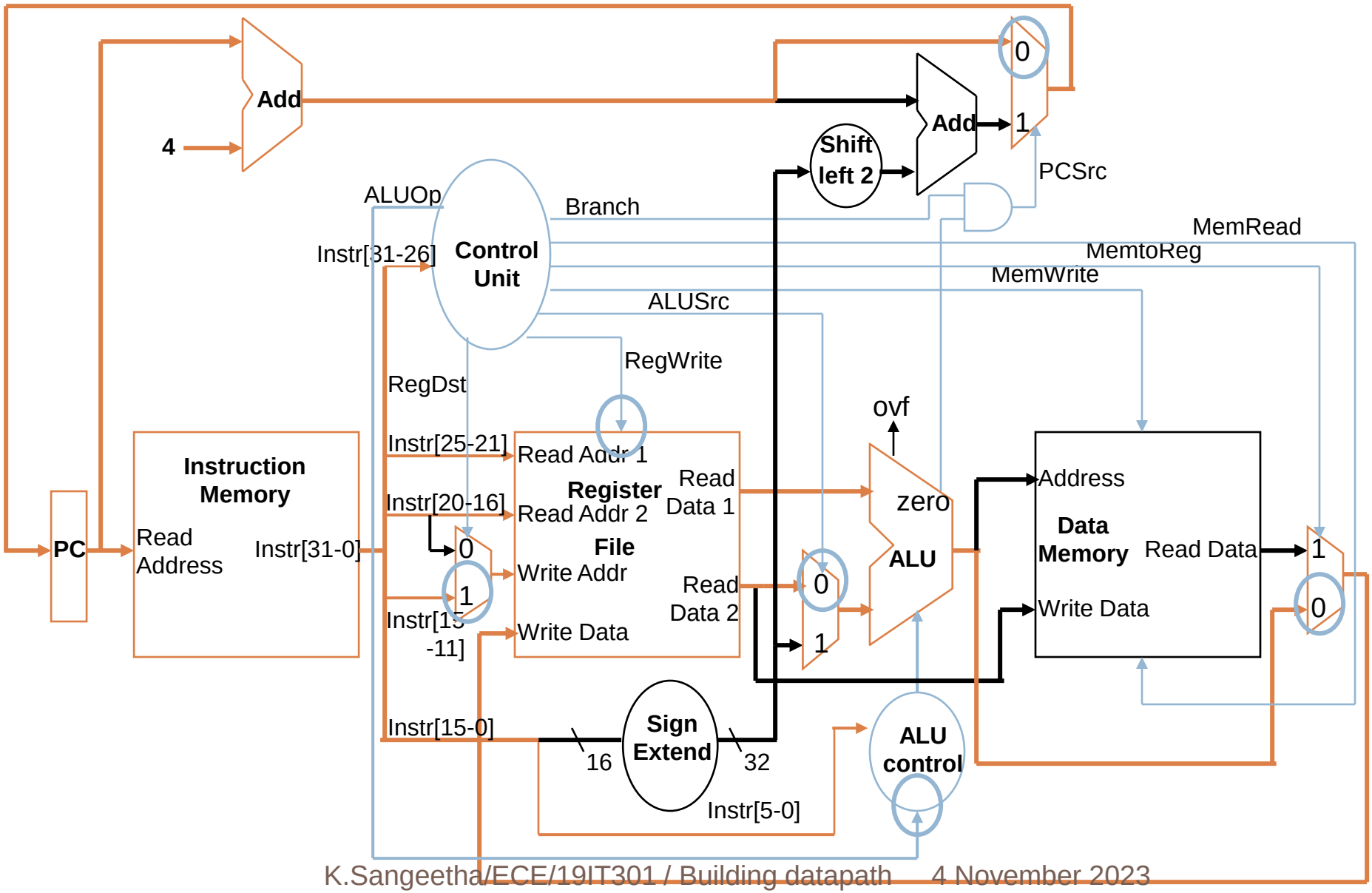
Adding the Control



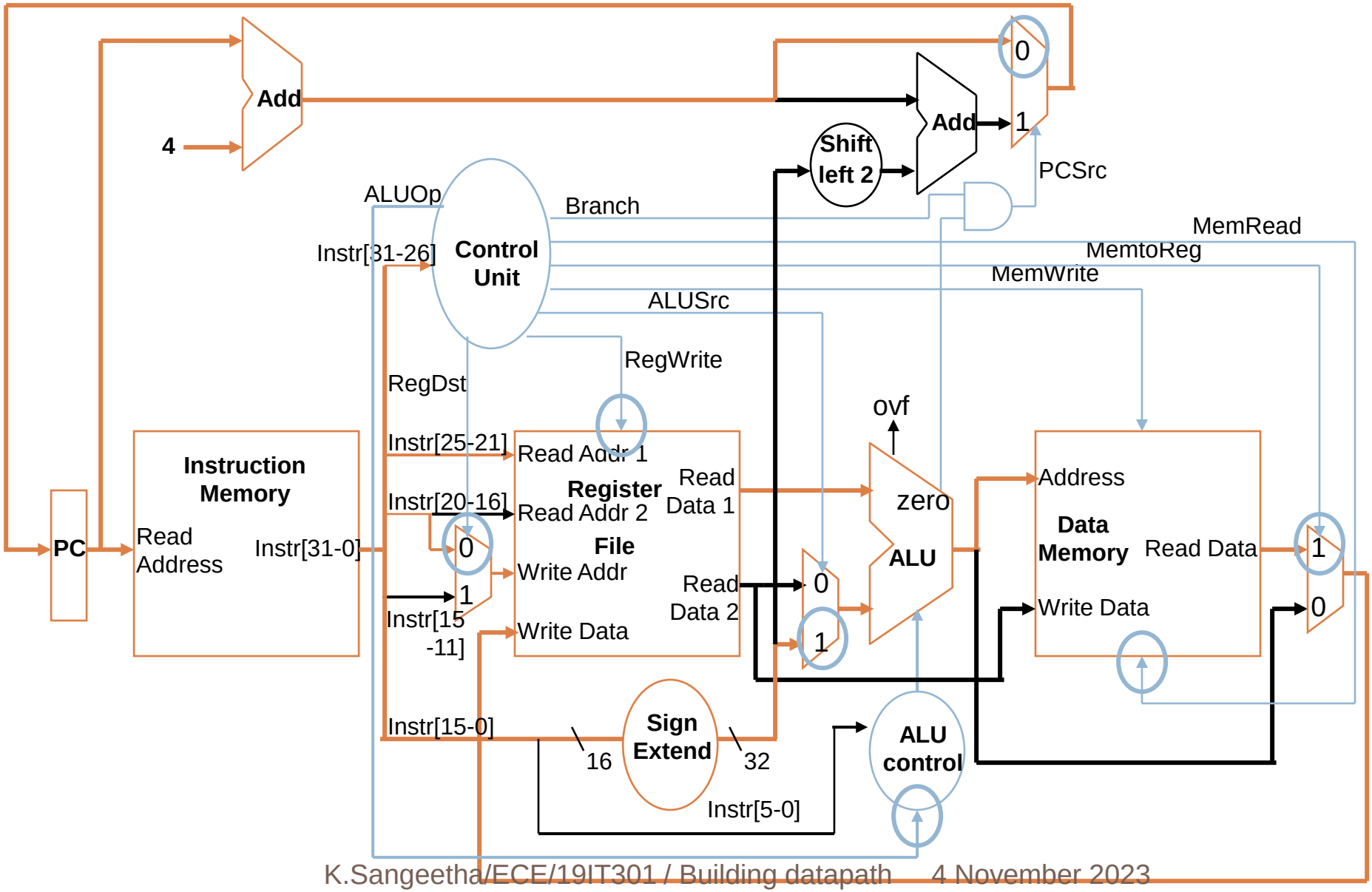
Single Cycle Datapath with Control Unit



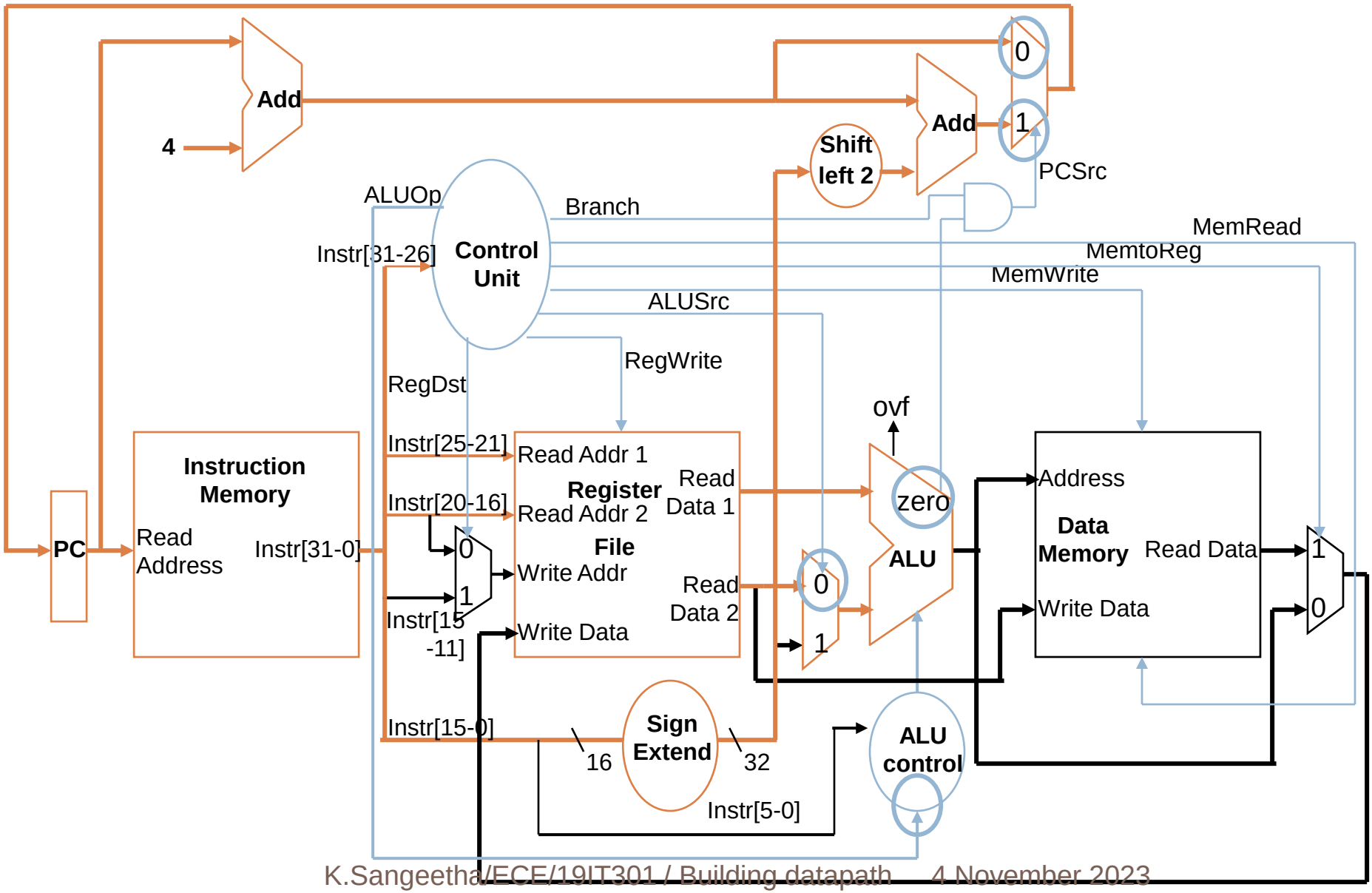
R-type Instruction Data/Control Flow



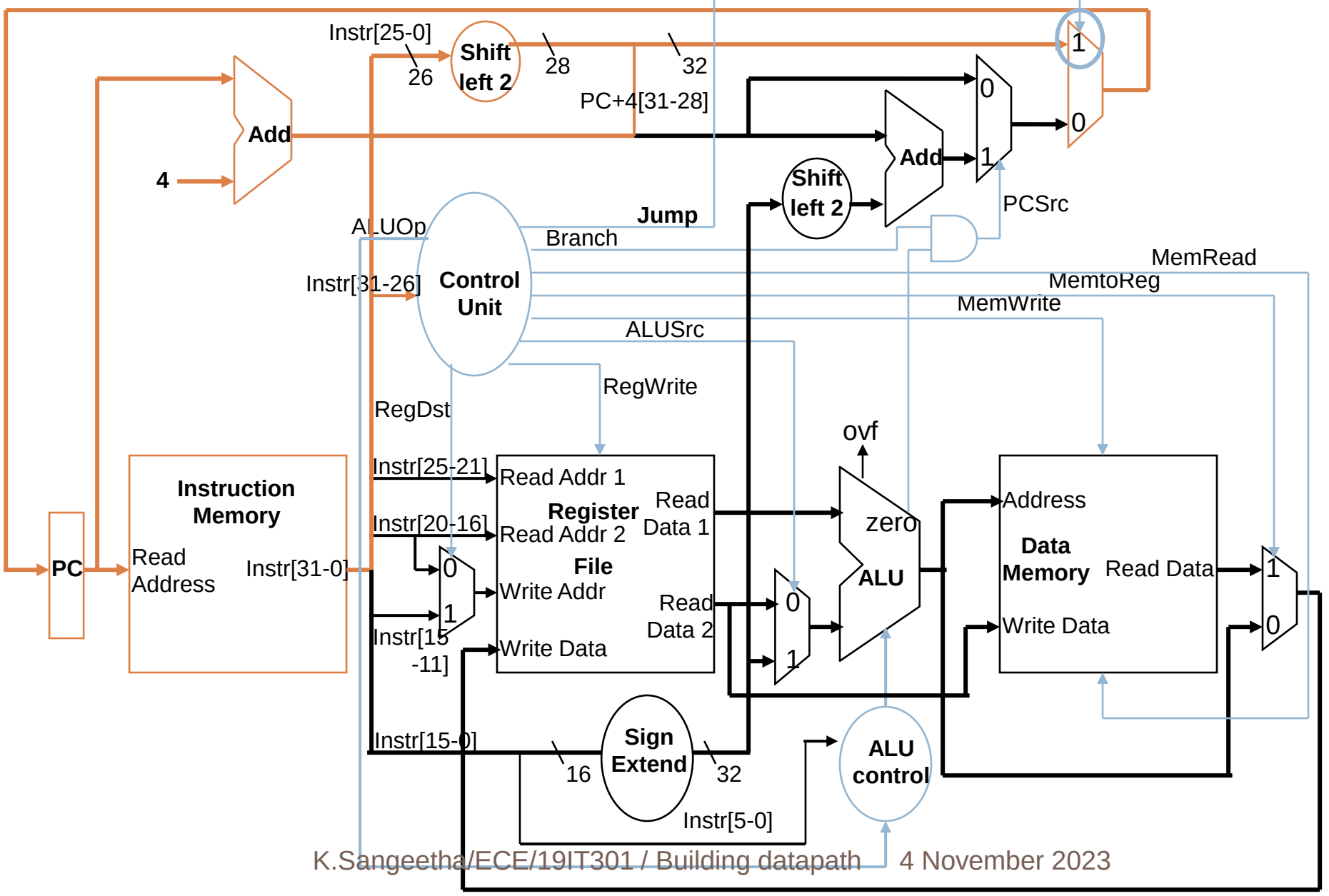
Load Word Instruction Data/Control Flow



Branch Instruction Data/Control Flow



Adding the Jump Operation



Upcoming….

ALU control lines	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	set-on-less-than
1100	NOR


Thank You