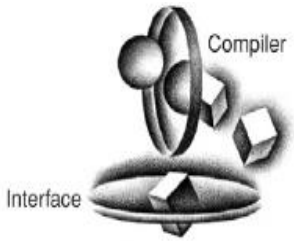
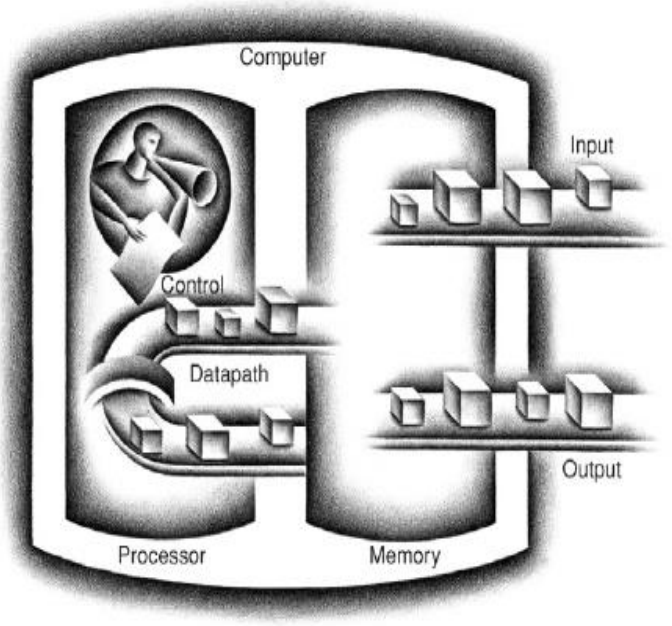
UNIT III PROCESSOR AND CONTROL UNIT

Basic MIPS implementation

Recall the Prior Knowledge

Introduction





CPU performance factors

- **Instruction count:** Determined by ISA and compiler
- **CPI and Cycle time :**Determined by CPU hardware

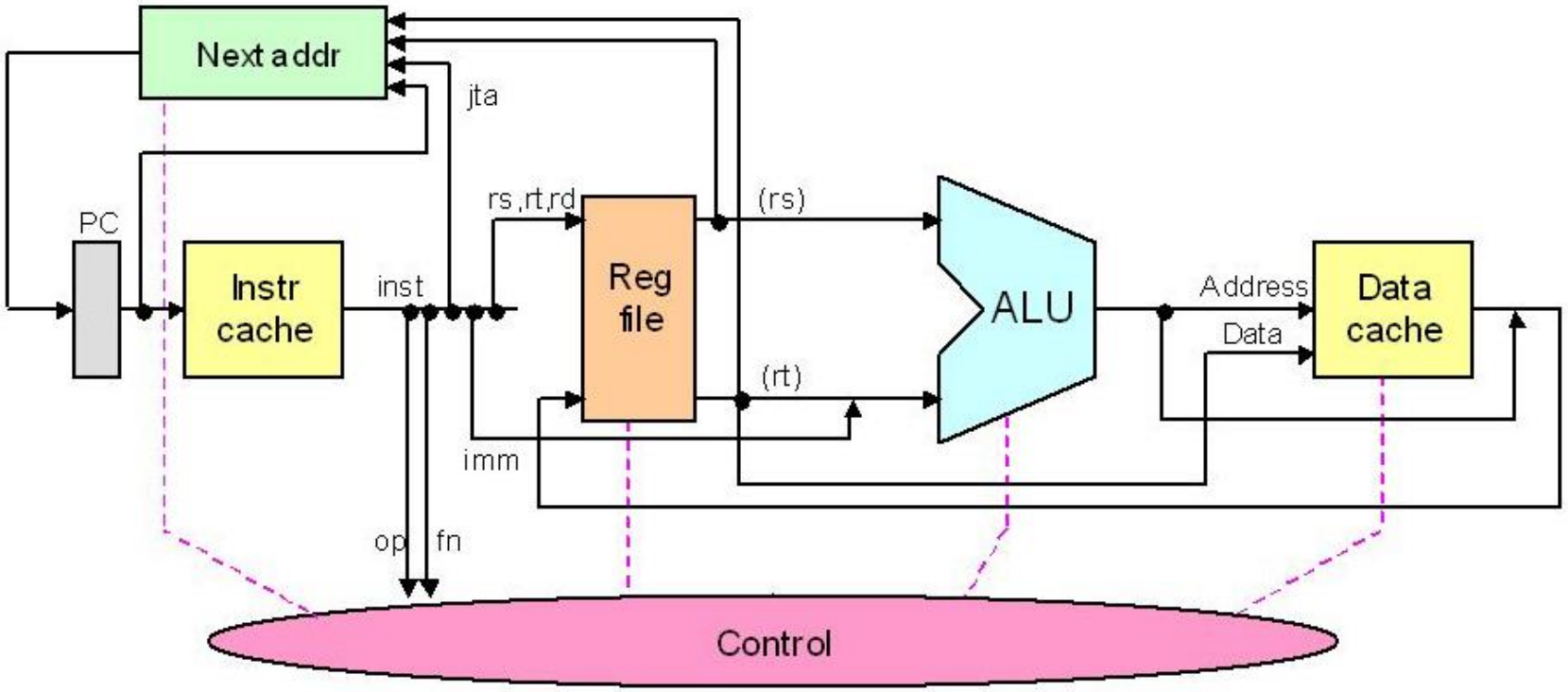
MIPS implementations

- **A simplified version**
- **A more realistic pipelined version**

Simple Subset

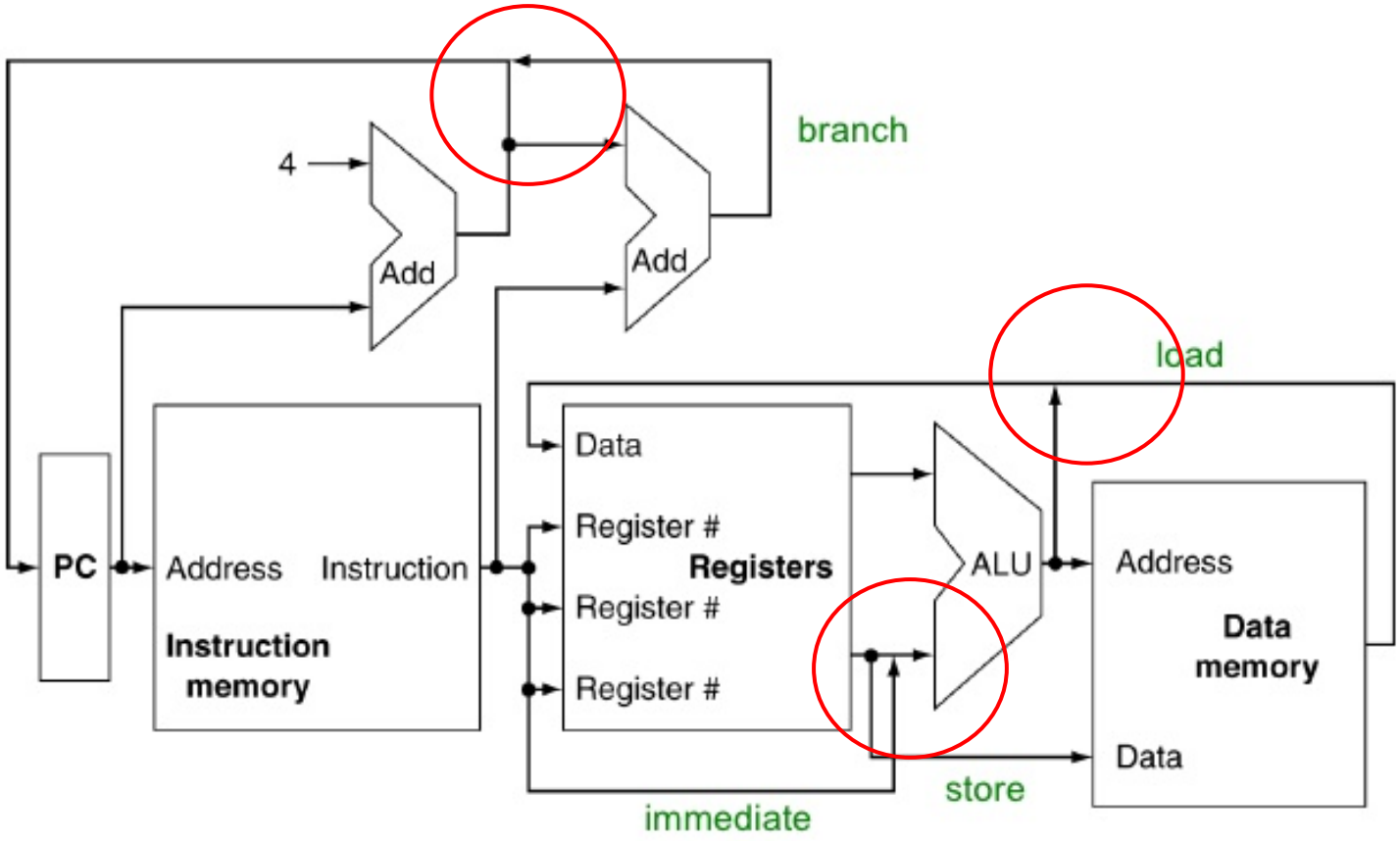
Memory reference: lw, sw
Arithmetic/logical: add, sub, and, or, slt
Control transfer: beq, j

Instruction Execution

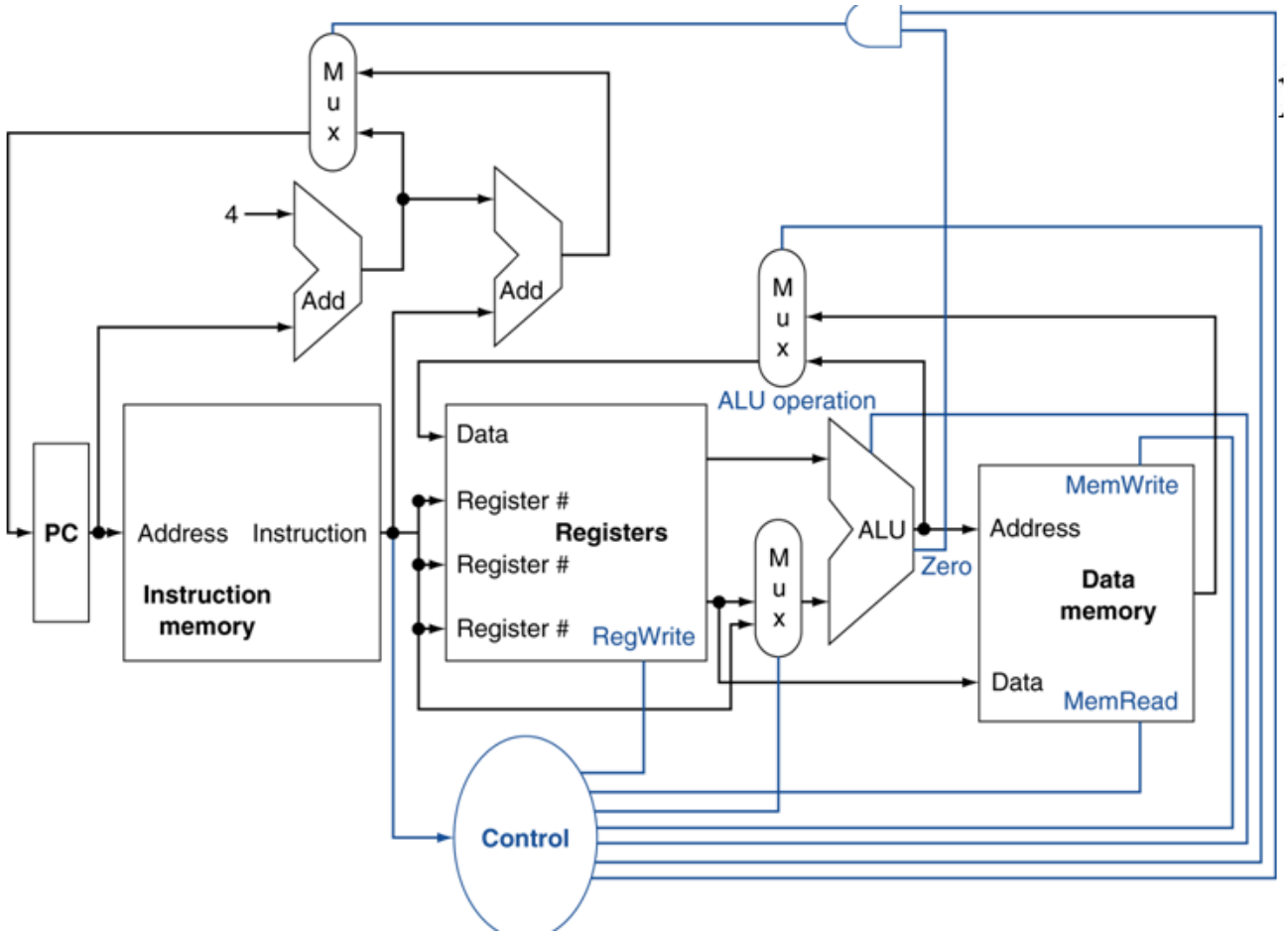


CPU Overview

Multiplexers



Control Signal

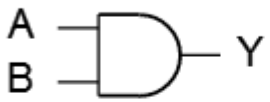


Logic Design Basics

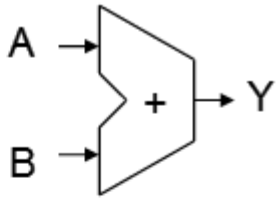
- Information encoded in binary
  - Low voltage = 0, High voltage = 1
  - One wire per bit
  - Multi-bit data encoded on multi-wire buses
- Combinational element
  - Operate on data
  - Output is a function of input
- State (sequential) elements
  - Store information

Combinational Elements

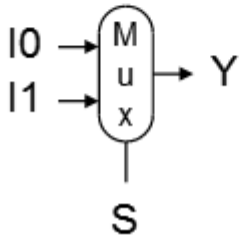
- AND-gate
  - Y = A & B



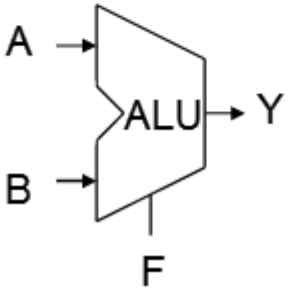
- Adder
  - Y = A + B



- Multiplexer
  - Y = S ? I1 : I0



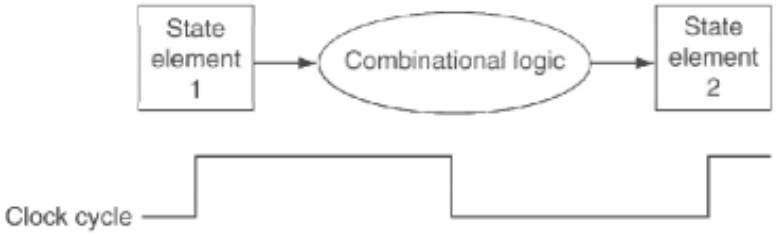
- Arithmetic/Logic Unit
  - Y = F(A, B)



Sequential Elements

- Register: stores data in a circuit
  - Uses a clock signal to determine when to update the stored value
  - Edge-triggered: update when Clk changes from 0 to 1

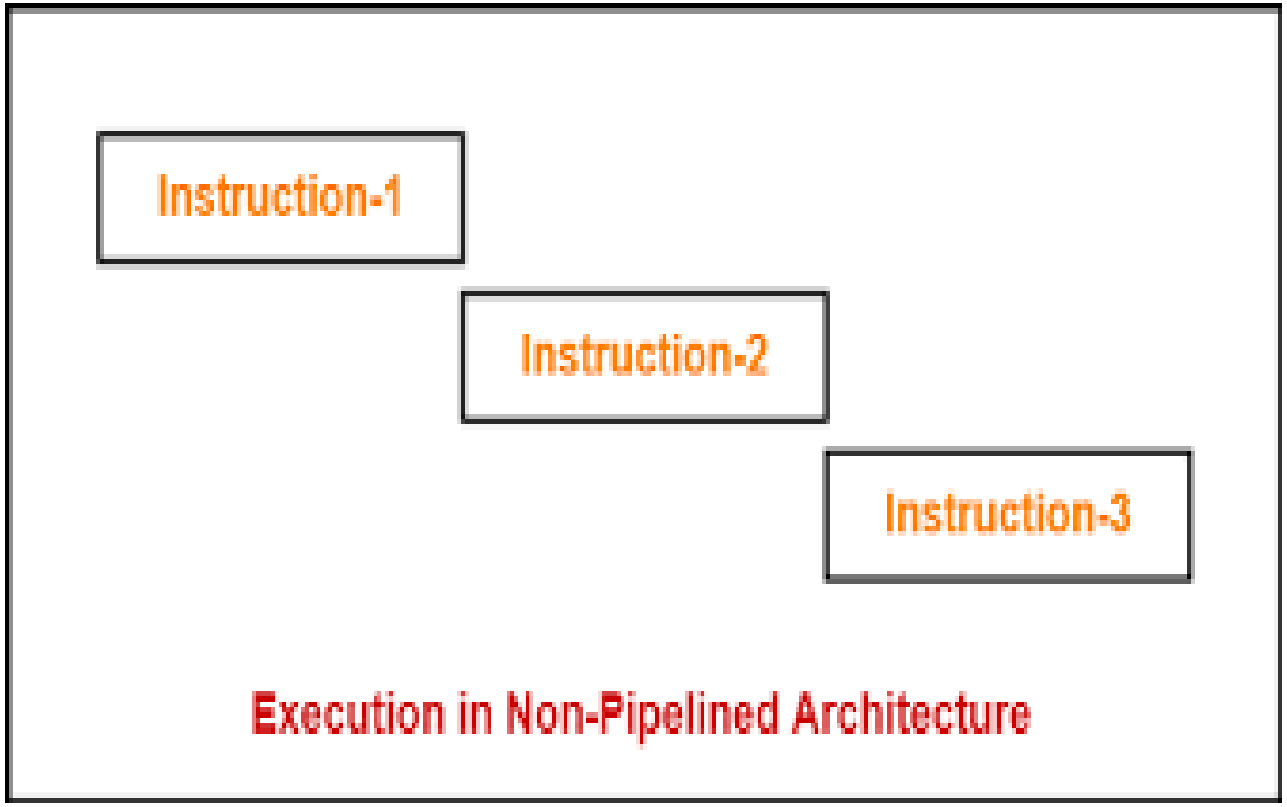
Clocking Methodology



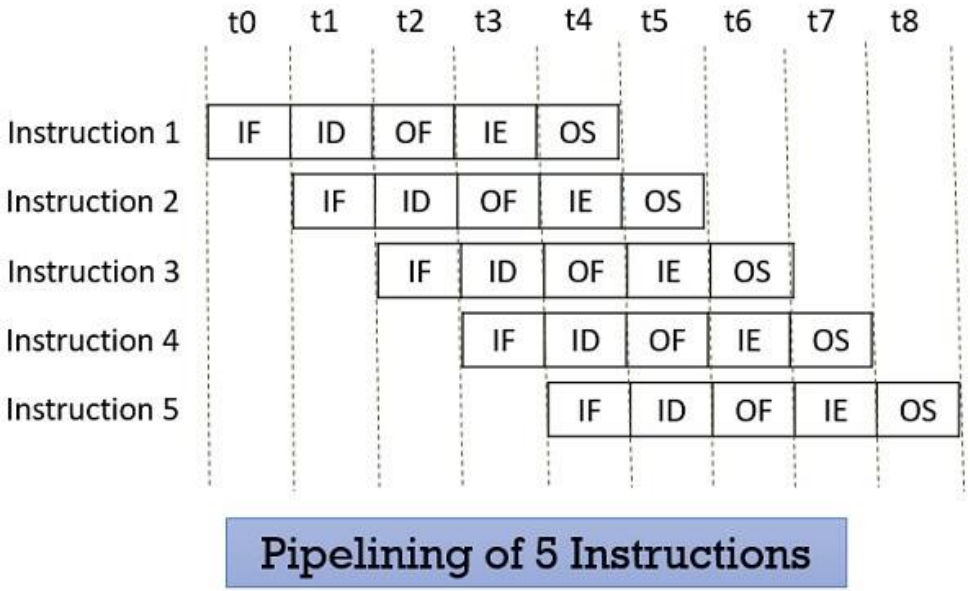
Combinational logic transforms data during clock cycles

- Between clock edges
- Input from state elements, output to state element
- Longest delay determines clock period

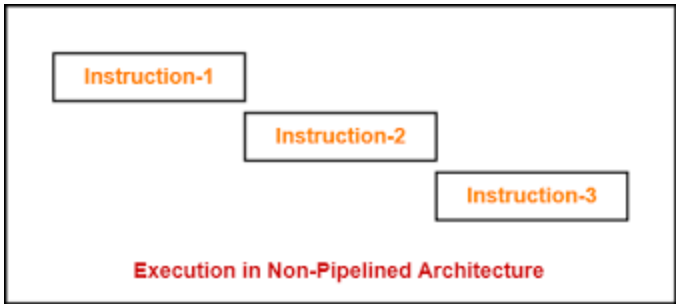
Upcoming


Instruction-1
Instruction-2
Instruction-3
Execution in Non-Pipelined Architecture

Upcoming



Pipelining of 5 Instructions




Thank You