SNS COLLEGE OF ENGINEERING

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE NAME : **19EC304 – ELECTRONIC CIRCUITS I**

II YEAR / III SEMESTER

Unit I- **BIASING OF DISCRETE BJT,FET**

Topic : Introduction to Need for biasing

Need for biasing

•Transistor biasing makes analog and digital operation of a transistor possible.
•Without transistor biasing, BJT amplifiers fail to deliver the required output across load terminals.
•The optimum value of transistor bias voltage is equal to two times the required AC output voltage peak. If you vary the transistor bias voltage, the Q-point will also shift its position.

Transistor Biasing and Operating Region

he Bipolar Junction Transistor (BJT) operates as either an analog device in applications such as amplifiers, oscillators, etc. or a digital device in converters and switching circuits. This dual action of the transistor is realized by transistor biasing.

The biasing applied to the two PN junctions of the transistor influences the movement of majority carriers and thus the behavior of the transistor. The biasing for a transistor to operate in an amplifier is entirely different from that in a transistor-based converter. Table.1 gives details about the region of operation and bias conditions at emitter and collector junctions when a transistor operates as an analog and digital device.

Transistor Operation		Transistor Bias		Region of operation
		Emitter Junction	Collector Junction	
Analog		FB	RB	Active
Digital	Switch in 'ON' state	FB	FB	Saturation
	Switch in 'OFF' state	RB	RB	Cut-off
Dormant		RB	FB	Inverted

Table.1 The region of operation and bias conditions in a transistor
**(FB-Forward Bias, RB- Reverse Bias)*

The biasing circuits for transistor switches are generally called base drive circuits. We are discussing transistor biasing in the context of a transistor amplifier.

Configuration	Transistor Terminals			Output = *f*(input)
	Common	Input	Output	
Common-Base (CB)	B	E	C	$I_c = f(I_E)$
Common-Emitter (CE)	E	B	C	$I_c = f(I_B)$
Common- Collector (CC)	C	B	E	$I_E = f(I_B)$

Transistor Amplifier

Let's catch a CE silicon NPN transistor amplifier (shown in Figure.1) in action. The E and C junctions can be supplied from a single dc voltage V_{cc} as it fulfills the major purpose of supplying the input transistor current. When an ac signal V_{in} is superimposed with the bias voltage V_{CC}, it similarly varies I_B with respect to time. The relationship given in Table.2 for the CE amplifier is obeyed and I_c follows the shape of I_B. The current gain denoted by in the transistor datasheet is the proportionality constant in the I_c - I_B relationship. The voltage drop I_CR_L gives the ac output voltage V_{out}.

Is Q-Point Susceptible to Transistor Bias Voltage?

How to place the Q-point in the middle of the active region? This can be implemented by adjusting I_B supplied by V_{cc} using a limiting resistor R_B inserted between V_{cc} and transistor base. The bias circuit is designed with two considerations:-

- I_B should remain somewhere in the middle of the active region even when AC swings due to V_{in} are introduced. This guarantees the steady and linear operation of the amplifier.
- The (V_{CE}, I_C) corresponding to these I_B swings should be within (V_{CE}, sat, $I_{C,\ sat}$) limits given in the transistor datasheet.

There are many combinations of (V_{CE}, I_C) satisfying the above criteria in a chosen I_B curve. Where exactly to fix the Q-point in this chosen I_B curve? This can be solved by drawing the DC-load line. The line connecting the maximum possible I_c and V_{CE} in the amplifier circuit is called the DC-load line.

Applying KVL to the output side of the amplifier (Figure.1) at dc bias conditions (C_c internal resistance ignored), we get

$V_{CE} = V_{cc} - I_C R_L$ (1)

The maximum possible I_C and V_{CE} are given by equations (2) and (3) respectively

$V_{CE, max} = V_{cc}$ at $I_C = 0$ (2)

$I_{C, max} = V_{cc}/R_L$ at $V_{CE} = 0$ (3)

The intersection of the dc-load line with the chosen I_B curve is the ideal Q-point for the faithful operation of your amplifier.
For a given amplifier, the Q-point shifts upwards with the rise in V_{cc} and vice-versa. Now, what is your inference about the Q-point of a transistor amplifier where V_{cc} is fluctuating continuously? Yes, exactly! We need a stabilized transistor biasing for distortionless amplification.

Any Query????

Thank you……