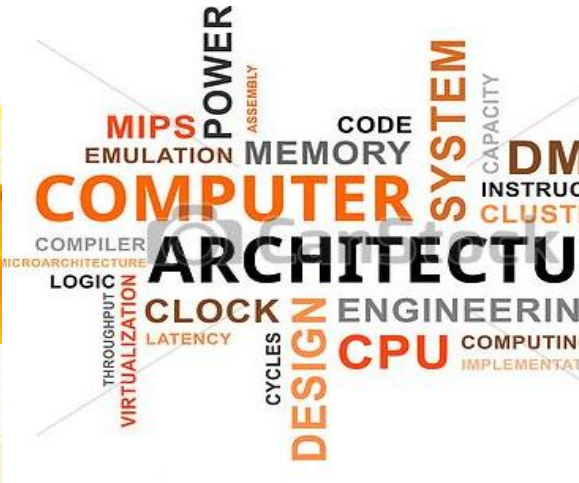
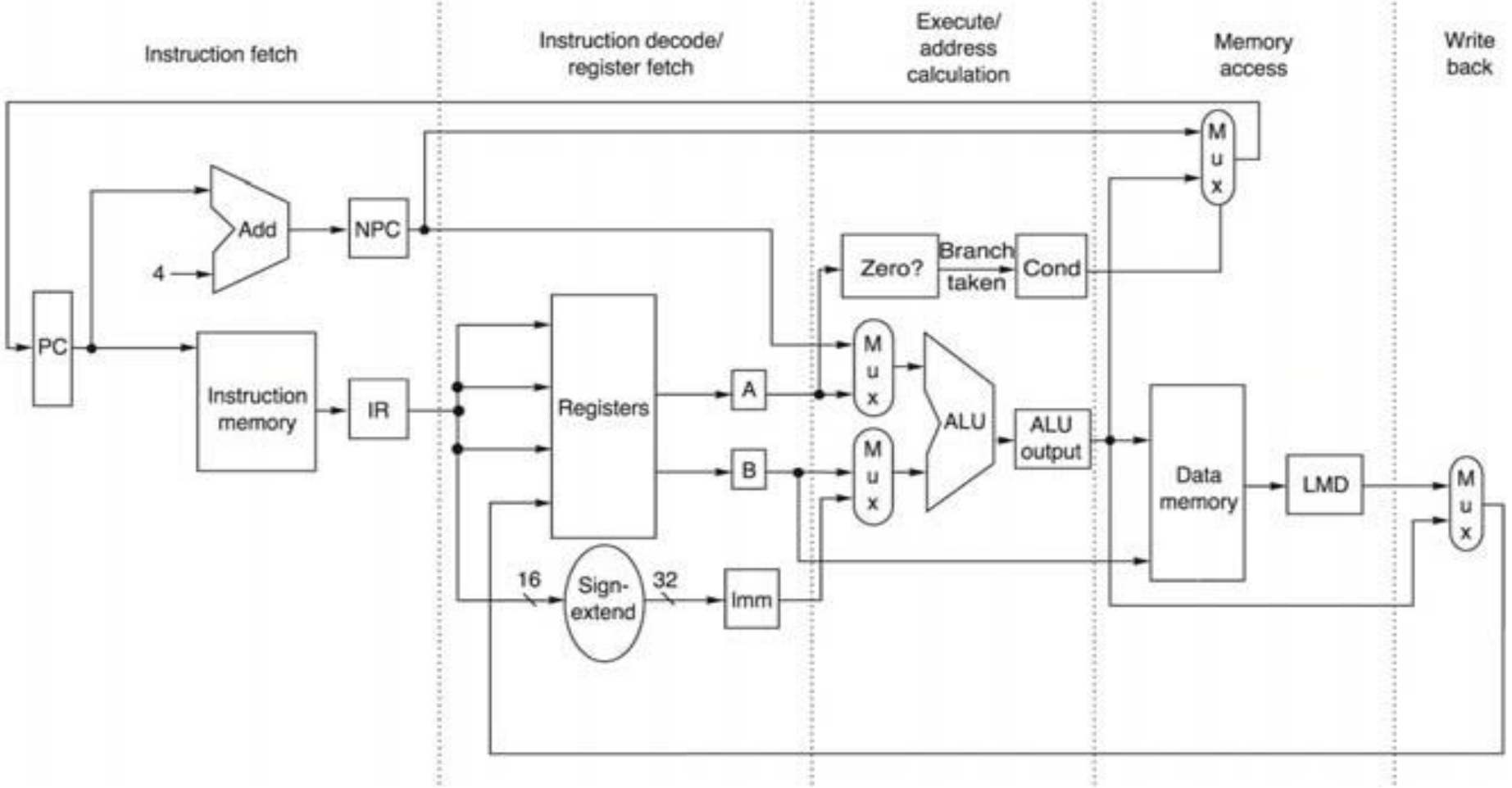
UNIT III
PROCESSOR AND PIPELINING

Fundamental concepts – Execution of a complete instruction – Multiple bus organization – Hardwired control – Micro programmed control – Pipelining: Basic concepts – Data hazards – Instruction hazards – **Influence on Instruction sets – Data path and control consideration.**

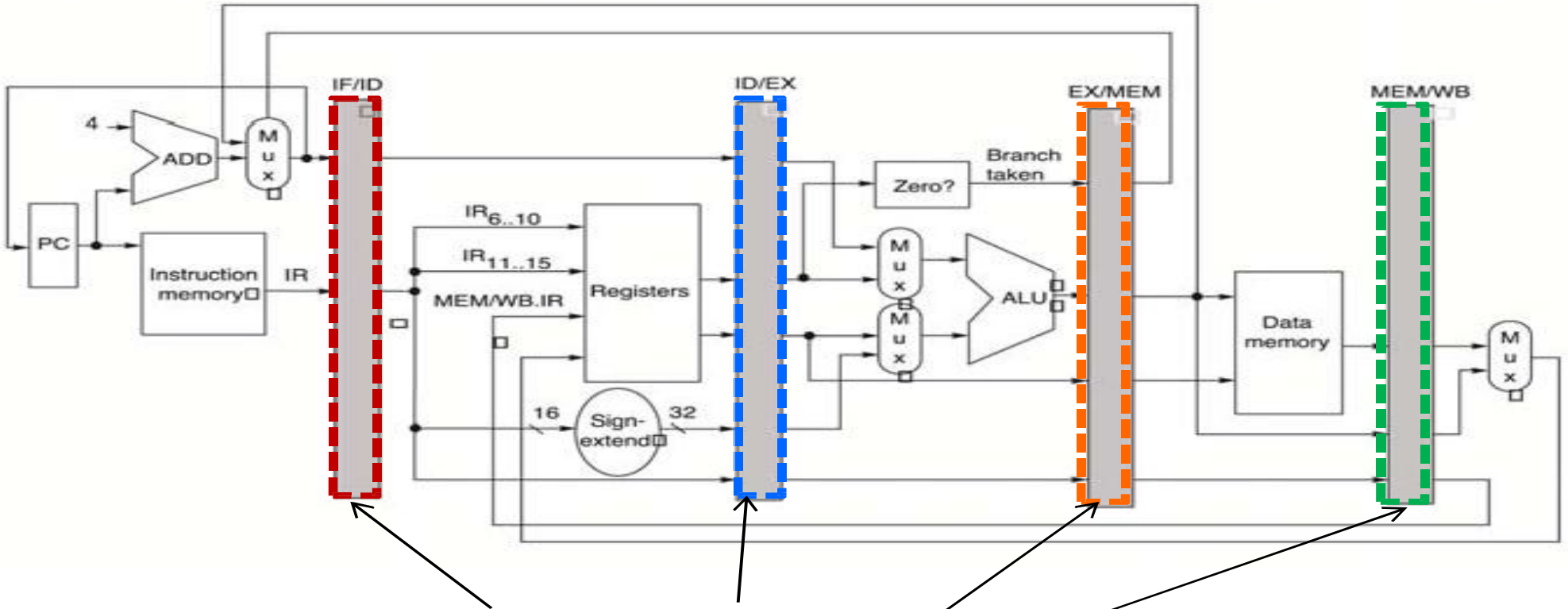


Recap the previous Class

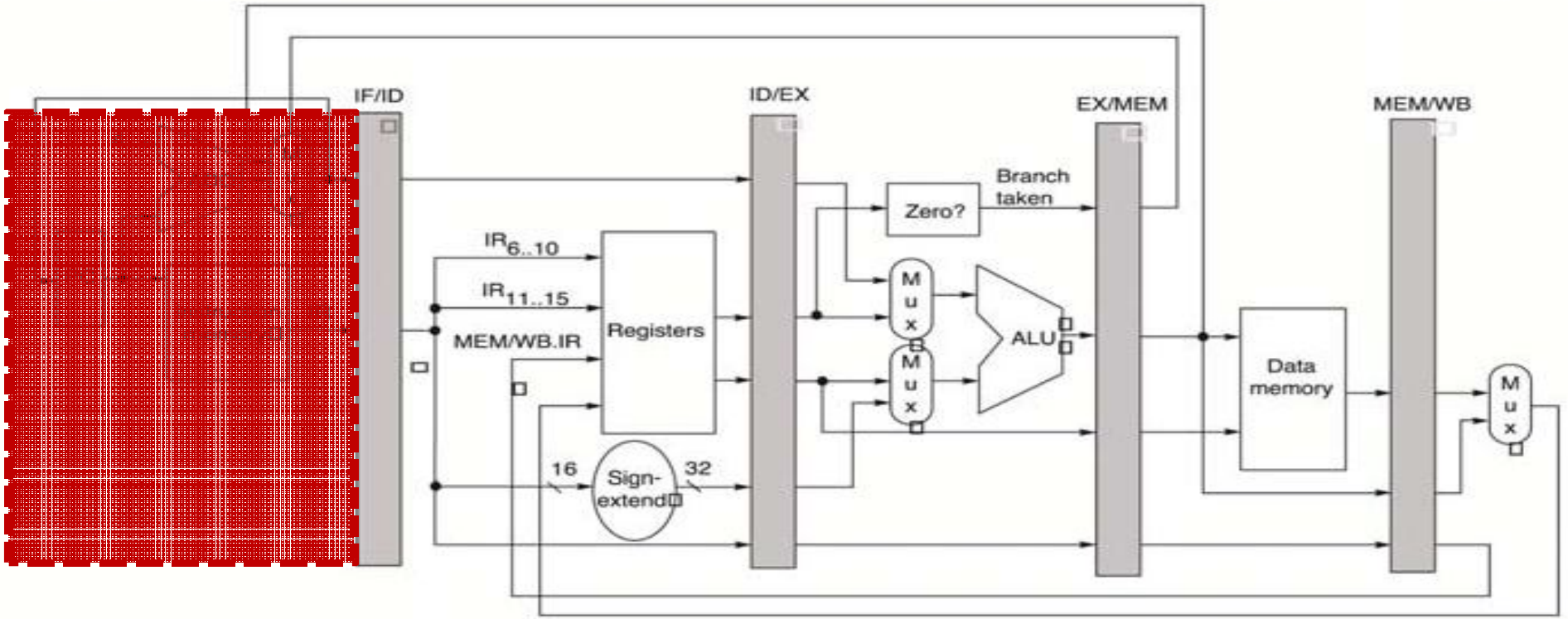
Multi-cycle to pipelined datapath



Multi-cycle to pipelined datapath

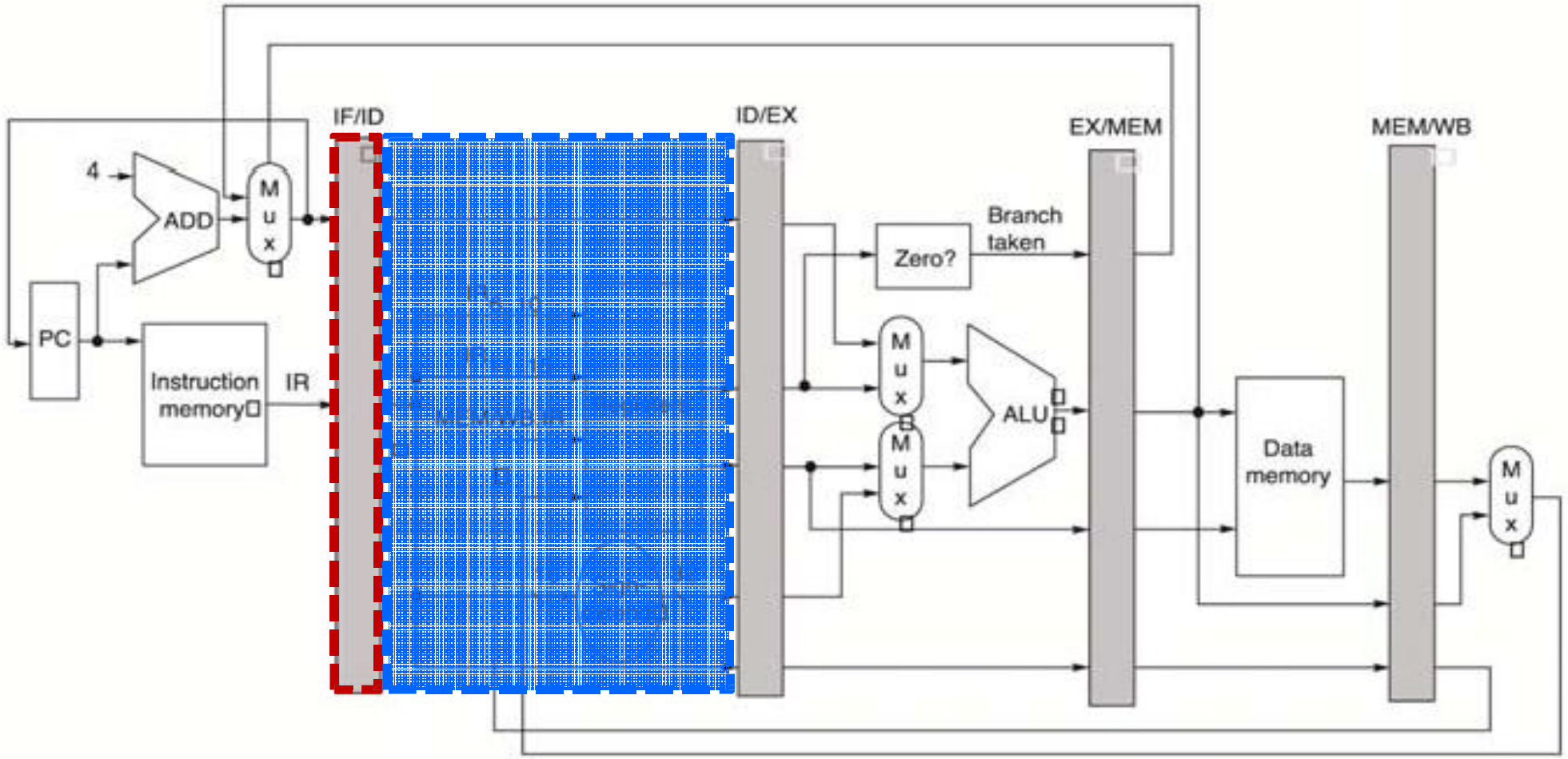


lw in the “F” stage



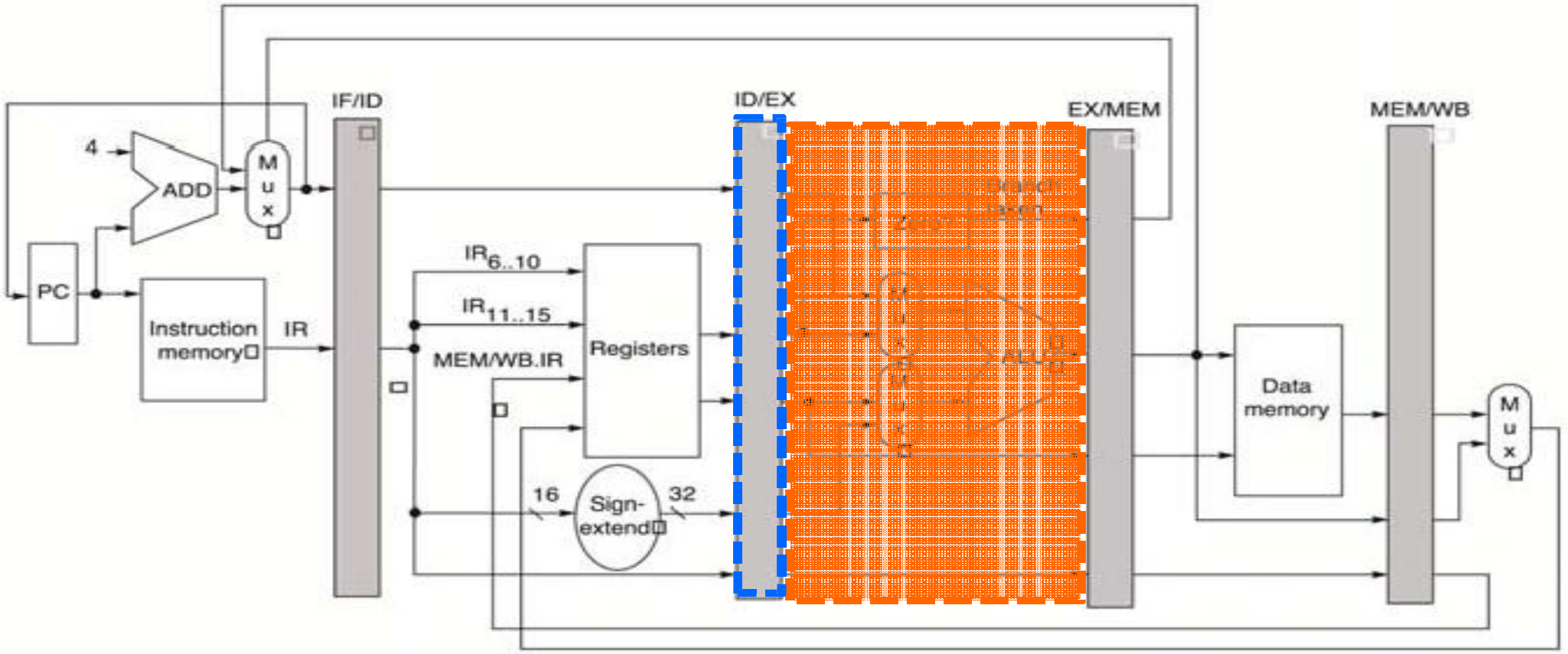
Read an instruction from instruction memory; address is in PC; compute (PC+4) to update PC

lw in the “D” stage



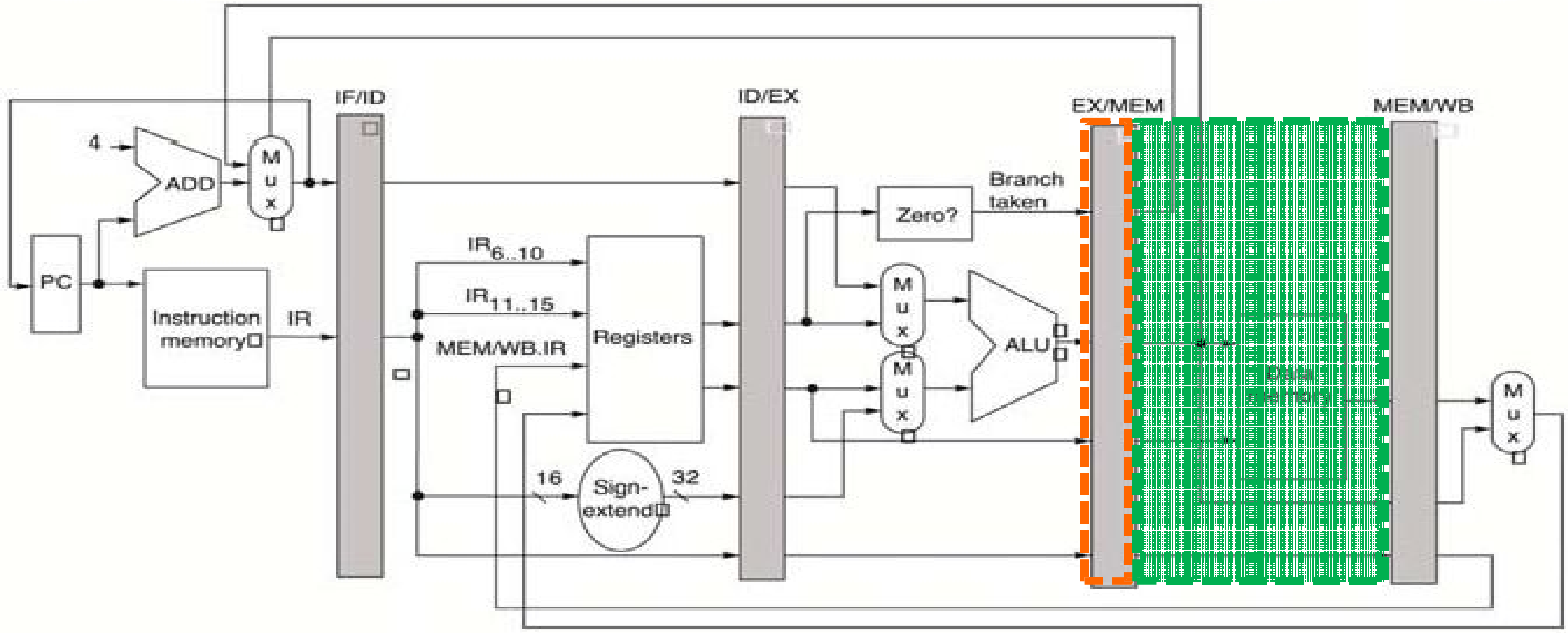
Read operands from register file; sign-extend the immediate field

lw in the “X” stage



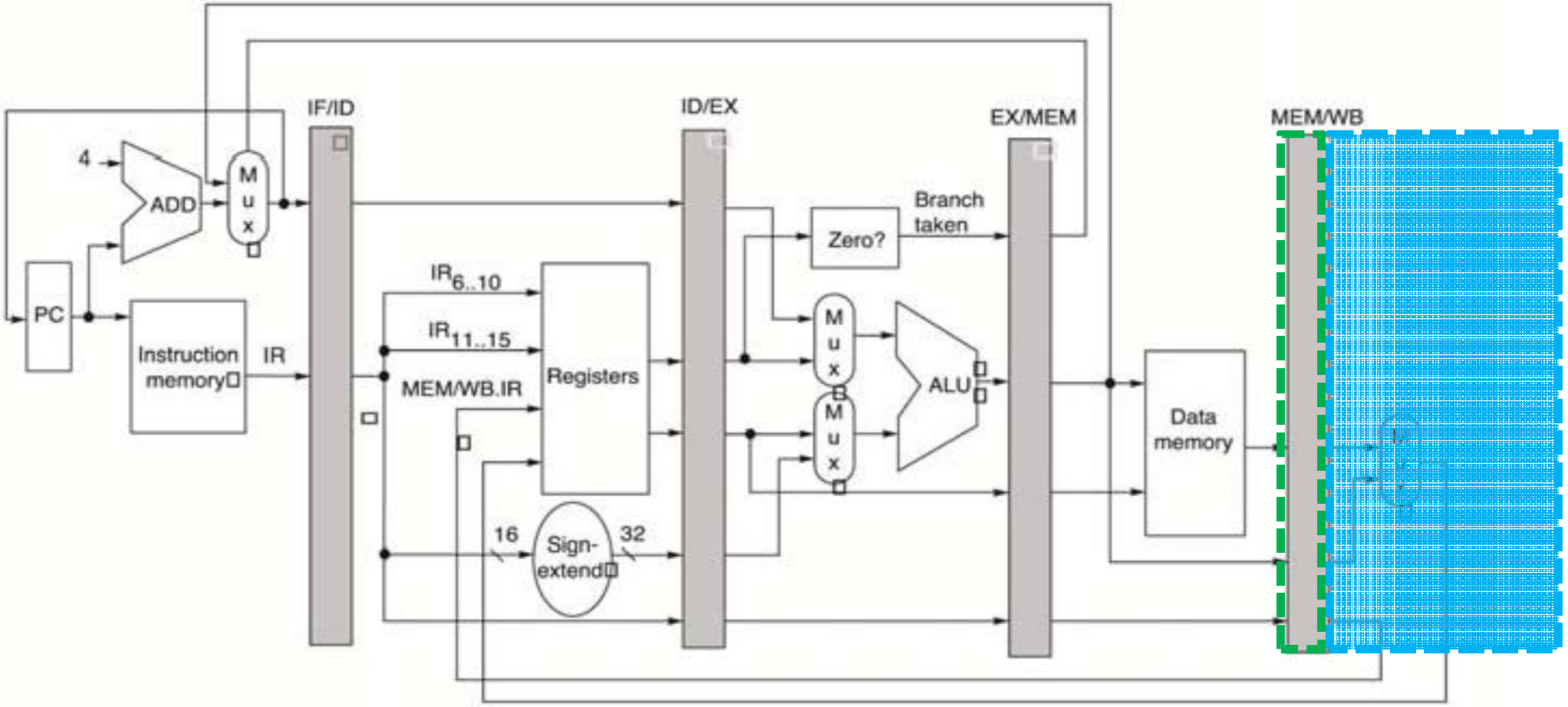
Add the base register value and the immediate value to form memory access address;

lw in the “M” stage



Read a value from memory

lw in the "W" stage

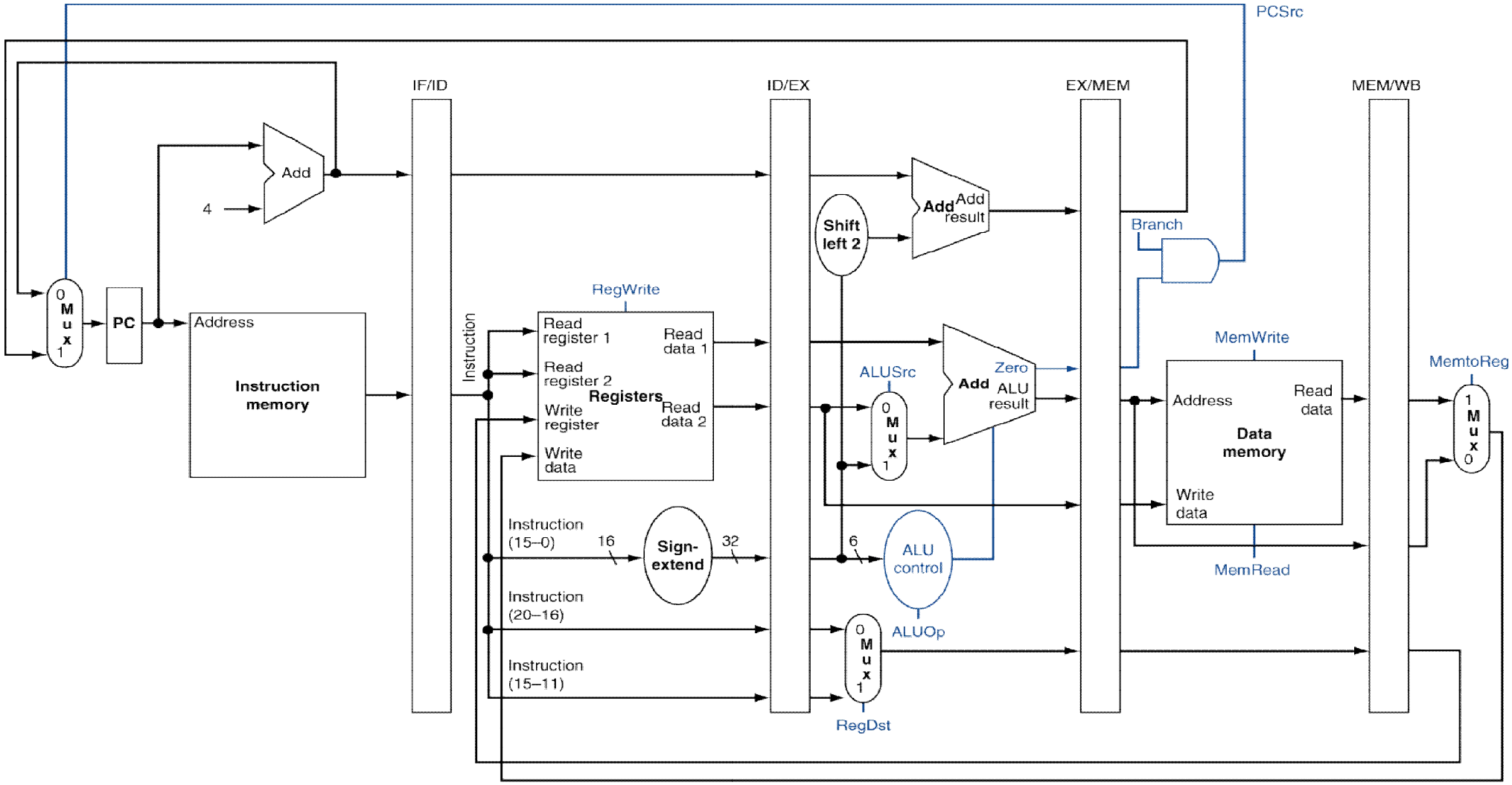


Update register file

Pipeline control

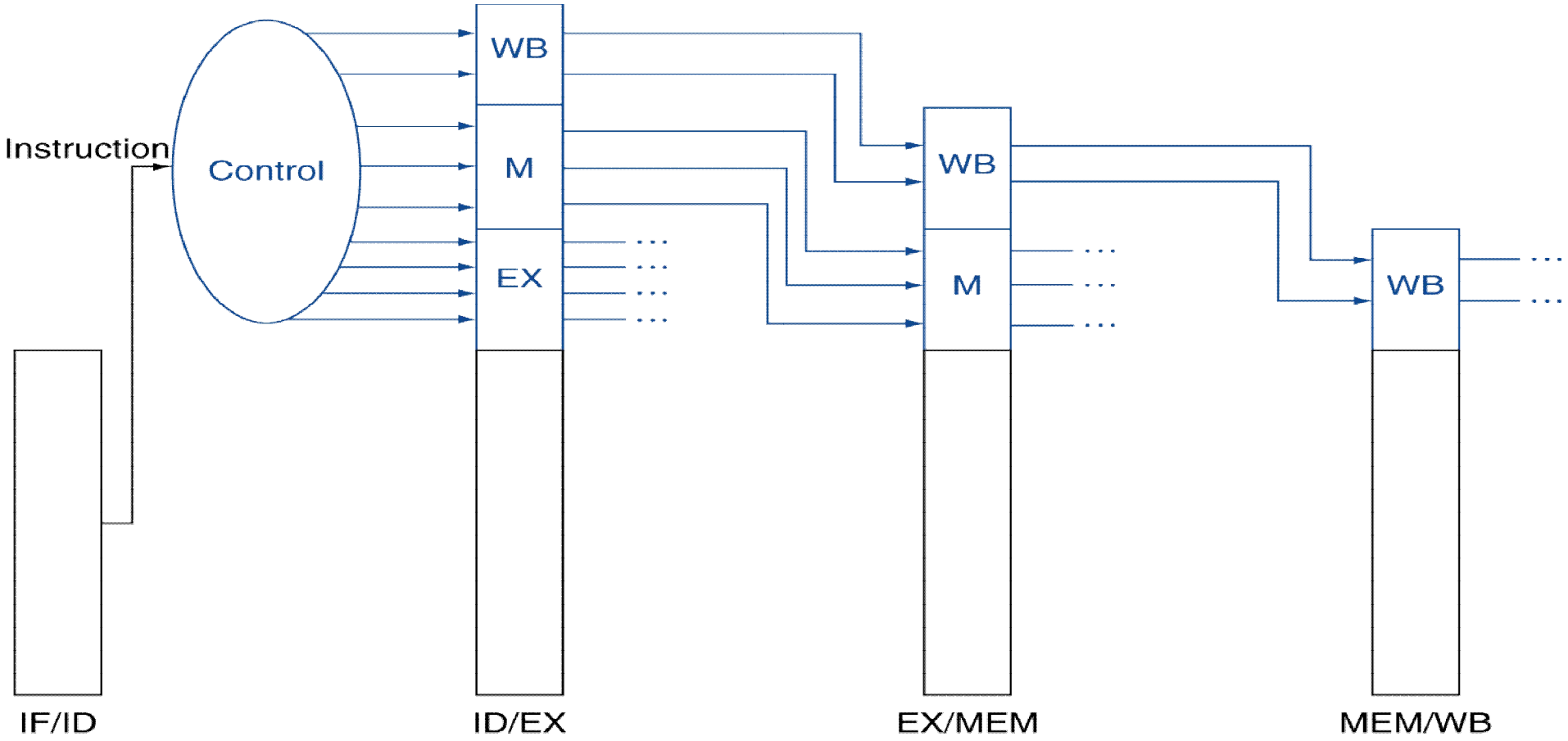
- There are multiple instructions in flight (in different pipeline stages)
- Hence, control signals for an instruction should flow through the pipeline stages with the instruction
- Alternatively, with the instruction information in each pipeline register, one can generate control signals by decoding the information
- Pipeline control becomes more complex than previous designs because of potential dependences between instructions in flight

Pipelined Control

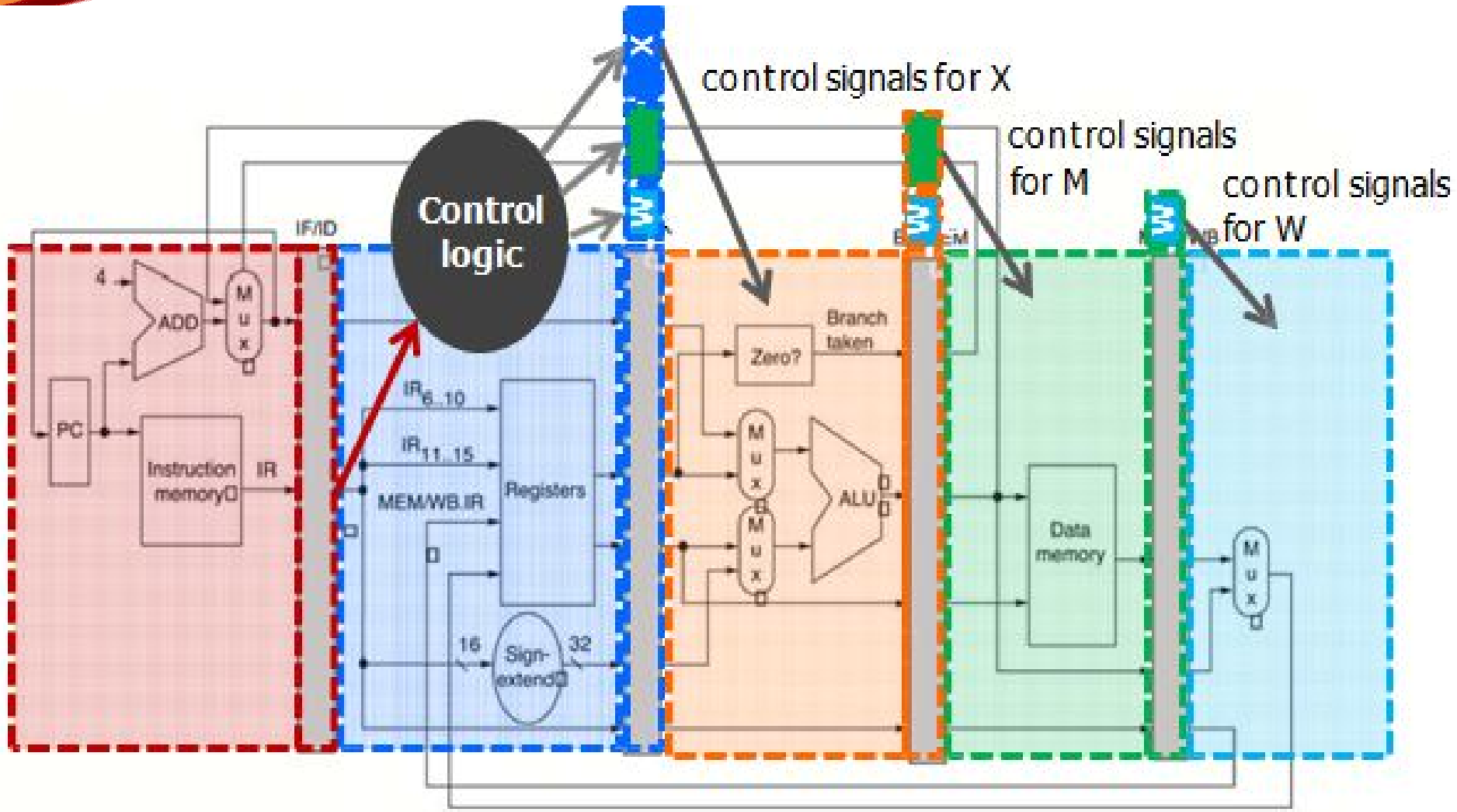


Pipelined Control

- Control signals derived from instruction
  - As in single-cycle implementation



Pipeline control



TEXT BOOK

Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.

REFERENCES

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3. John P.Hayes, “Computer Architecture and Organization”, McGraw Hill, 3rd Edition, 2002
4. M. Morris R. Mano “Computer System Architecture” 3rd Edition 2007
5. David A. Patterson “Computer Architecture: A Quantitative Approach”, Morgan Kaufmann; 5th edition 2011

Courtesy : **University of Pittsburgh**

THANK YOU