SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

16EC303–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT III-SEQUENTIAL LOGIC CIRCUITS

TOPIC 1-STATIC LATCHES AND DYNAMIC REGISTERS

OUTLINE

- LATCH VERSUS REGISTER
- LATCH-BASED DESIGN
  - MUX,
  - MASTER SLAVE REGISTER
- ACTIVITY
- TIME,CLK BASED LATCHES
- PULSE-TRIGGERED LATCHES
- SUMMARY

Introduction – Latches and Registers

REGISTER

- Used to hold the system state. Clock pulse is applied to the registers. On the rising edge of the clock pulse, the next state bits are copied to the output of the registers **.**

Two Types

1. **Positive edge triggered –** input is copied on positive edge of clock.
2. **Negative edge triggered -** input is copied on negative edge of clock**.**

LATCH

- Level sensitive circuit which is used to pass the D input to the Q output when clock is high**.**

SET UP TIME

- Time during which the data input is valid before the transition of the clock pulse.

HOLD TIME

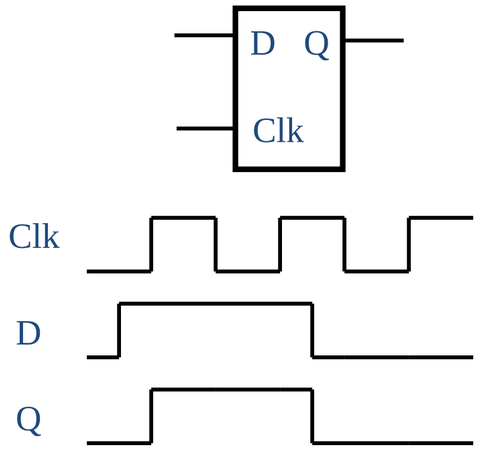
- Time during which the data input remains valid after the edge of the clock pulse.

CONTAMINATION DELAY – Minimum Delay

LATCH VERSUS REGISTER

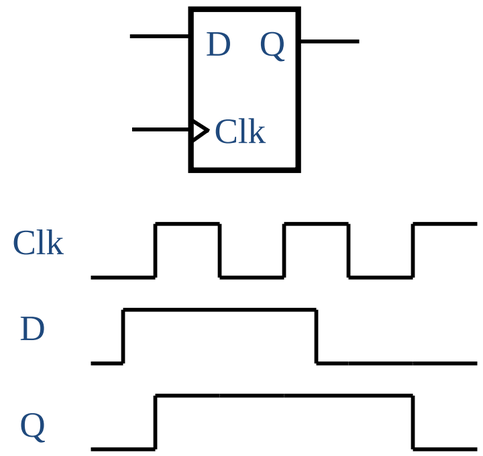
- Latch

  stores data when clock is low

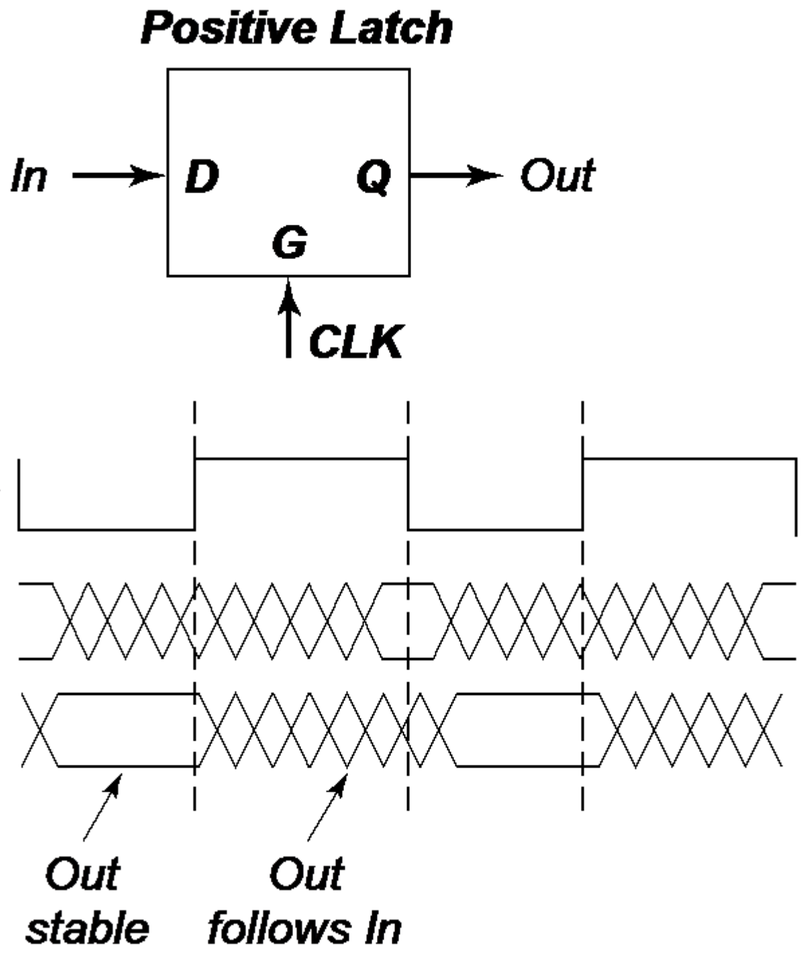


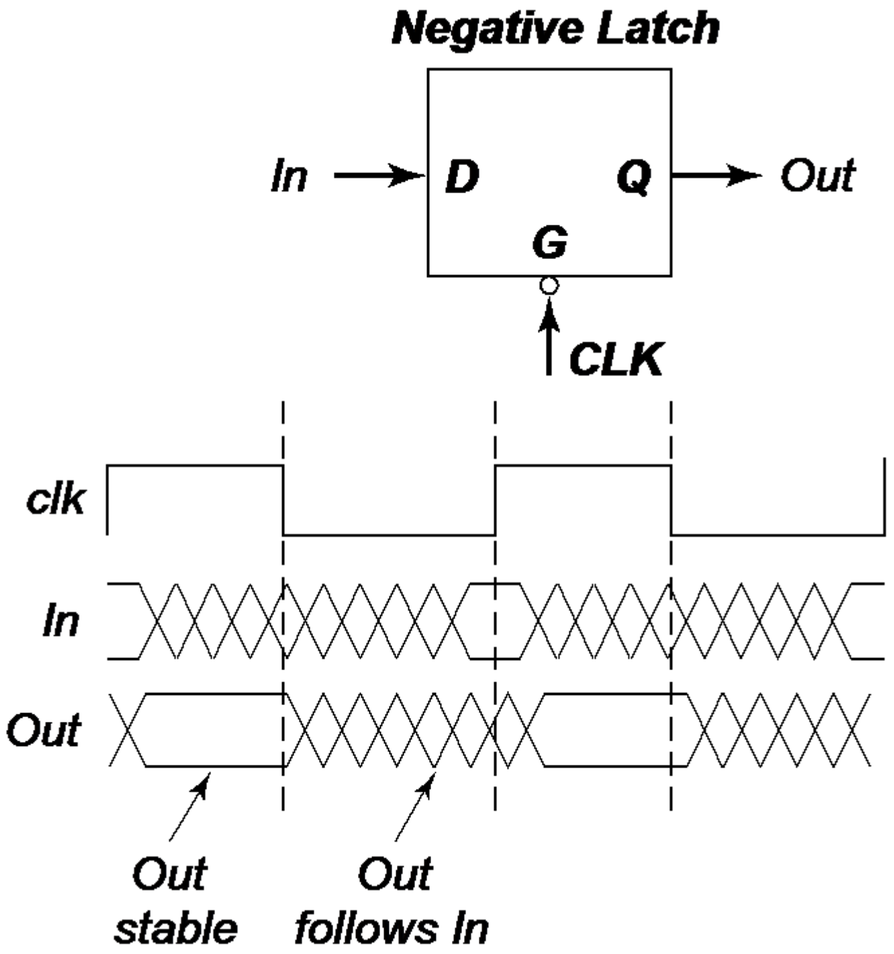
- Register

  stores data when clock rises



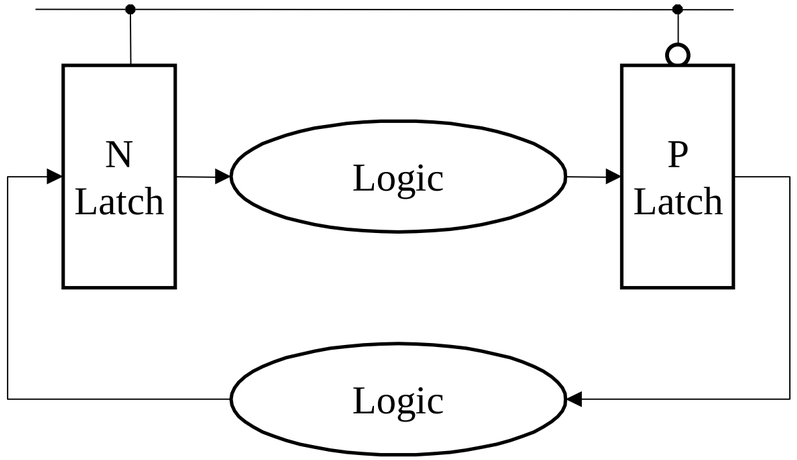
LATCHES


Positive Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In

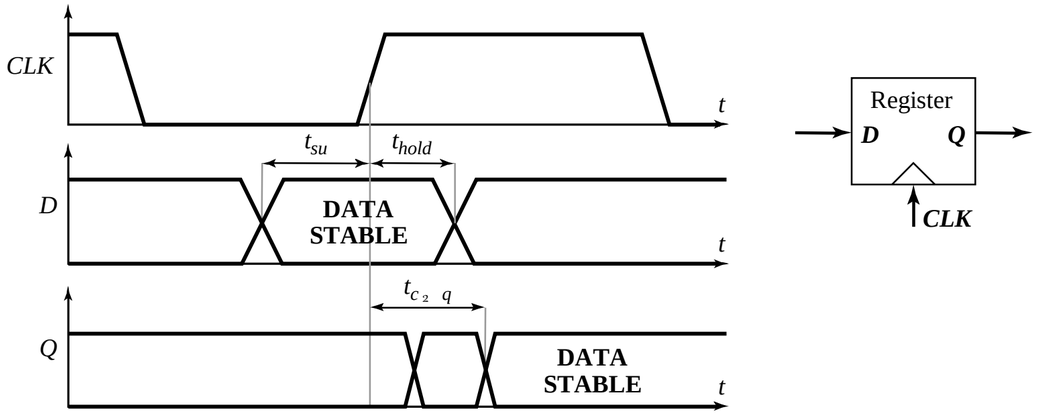

Negative Latch
In
D
Q
Out
G
CLK
clk
In
Out
Out stable
Out follows In

LATCH-BASED DESIGN

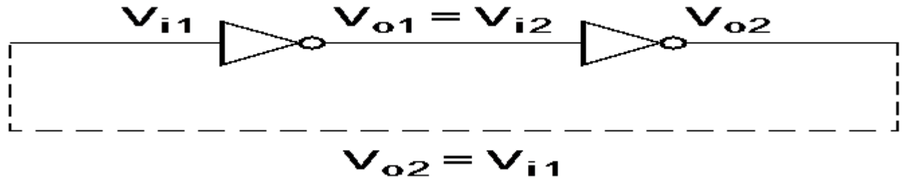
- N latch is transparent when f = 0
- P latch is transparent when f = 1

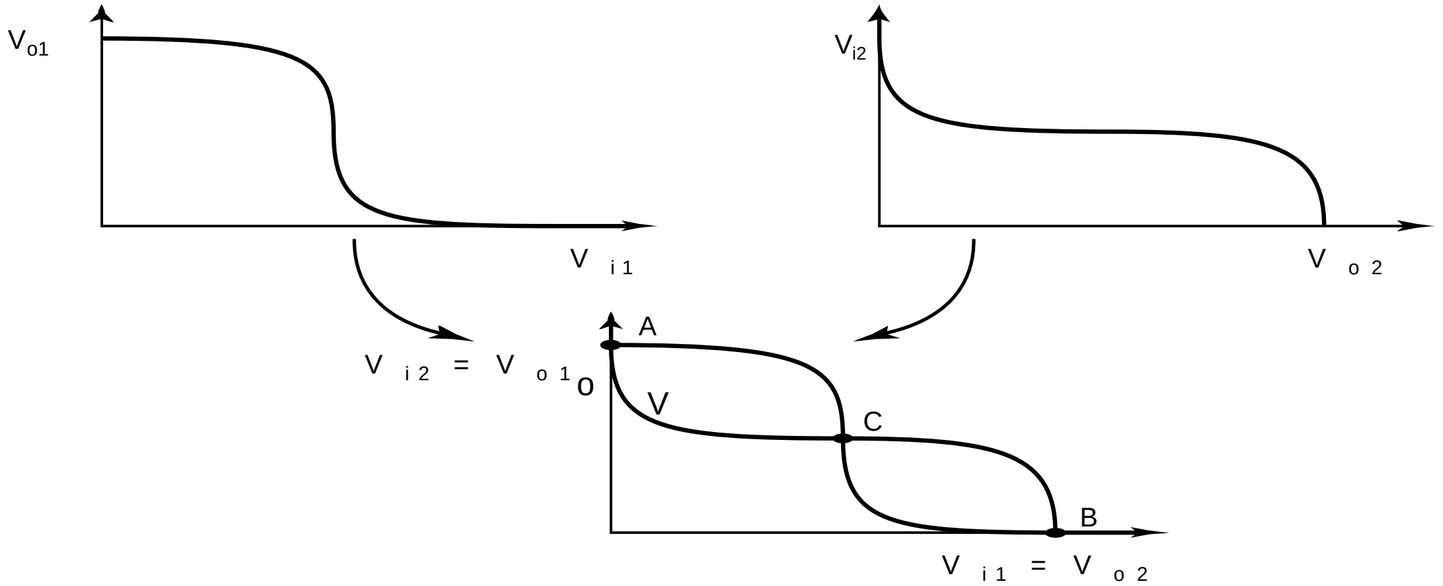


TIMING DEFINITIONS

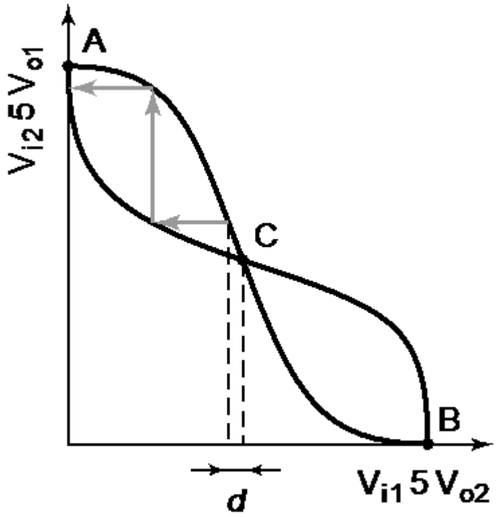


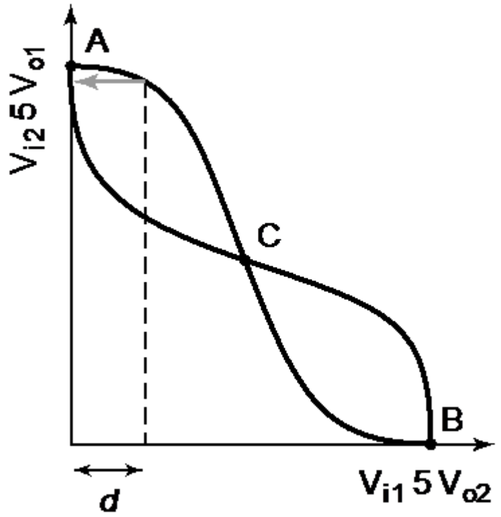
POSITIVE FEEDBACK: BI-STABILITY





META-STABILITY

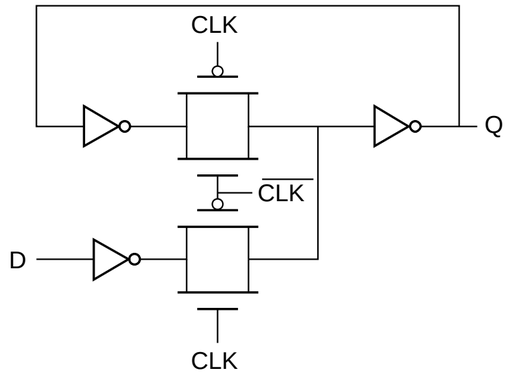




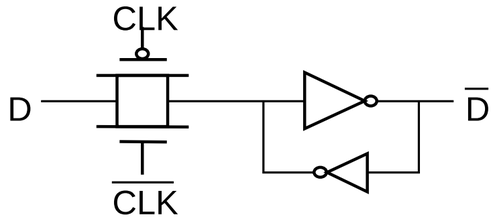
Gain should be larger than 1 in the transition region

WRITING INTO A STATIC LATCH

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states

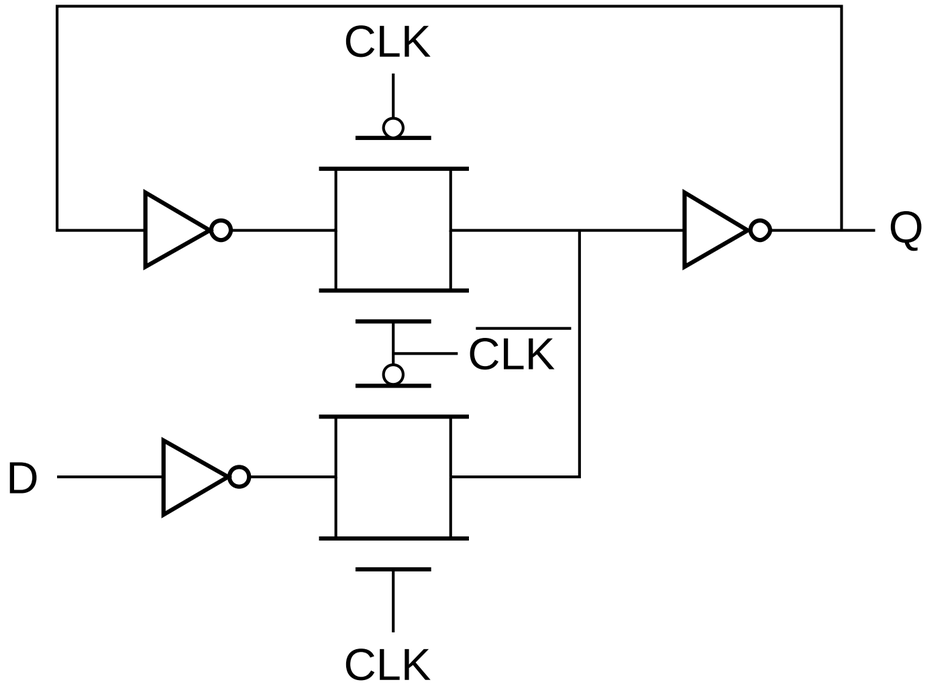


Converting into a MUX



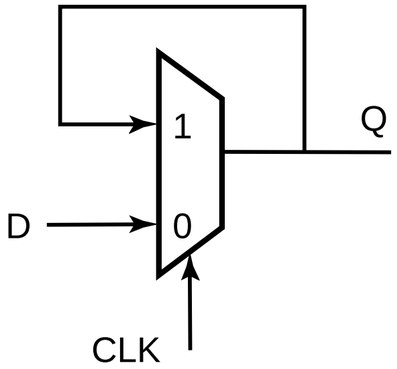
Forcing the state
(can implement as NMOS-only)

MUX-BASED LATCH



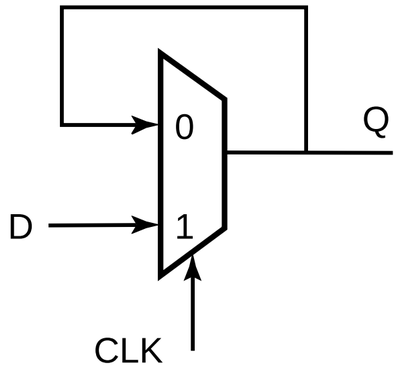
MUX-BASED LATCHES

Negative latch
(transparent when CLK= 0)



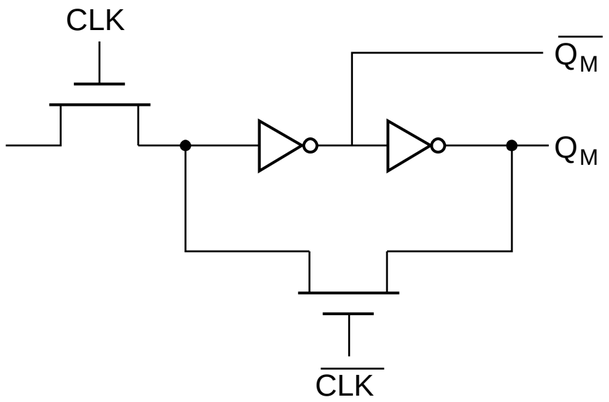
$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Positive latch
(transparent when CLK= 1)

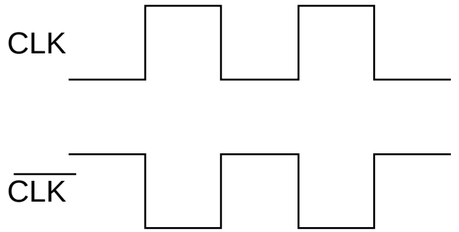


$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

MUX-BASED LATCH

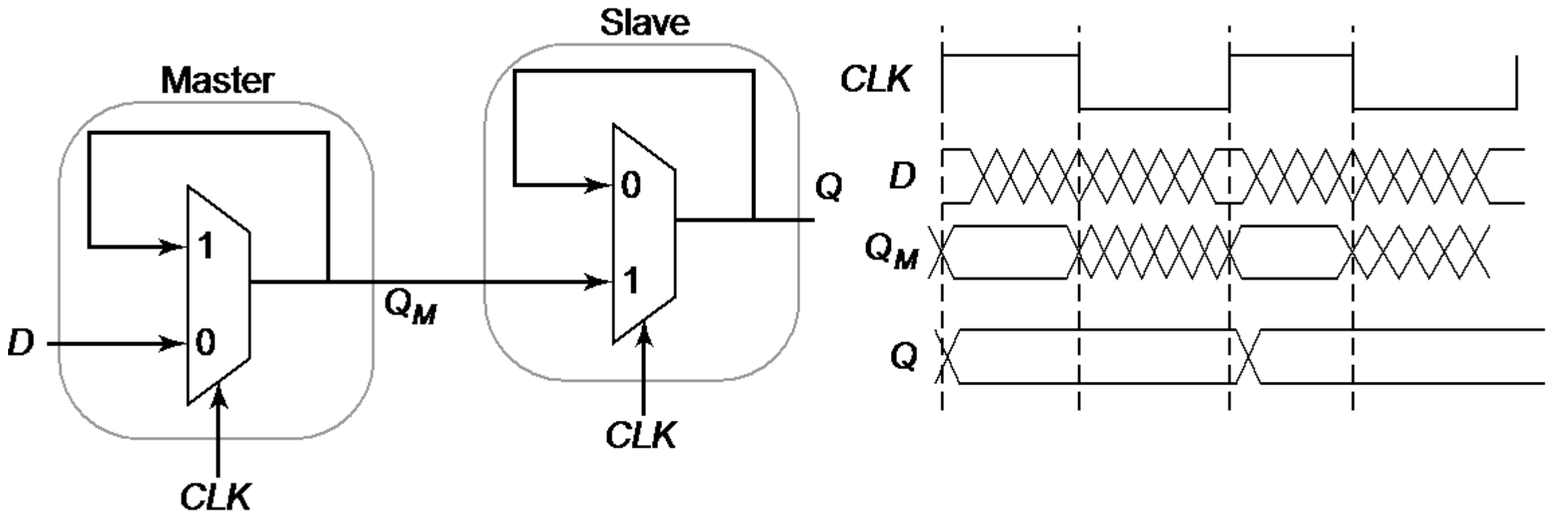


NMOS only



Non-overlapping clocks

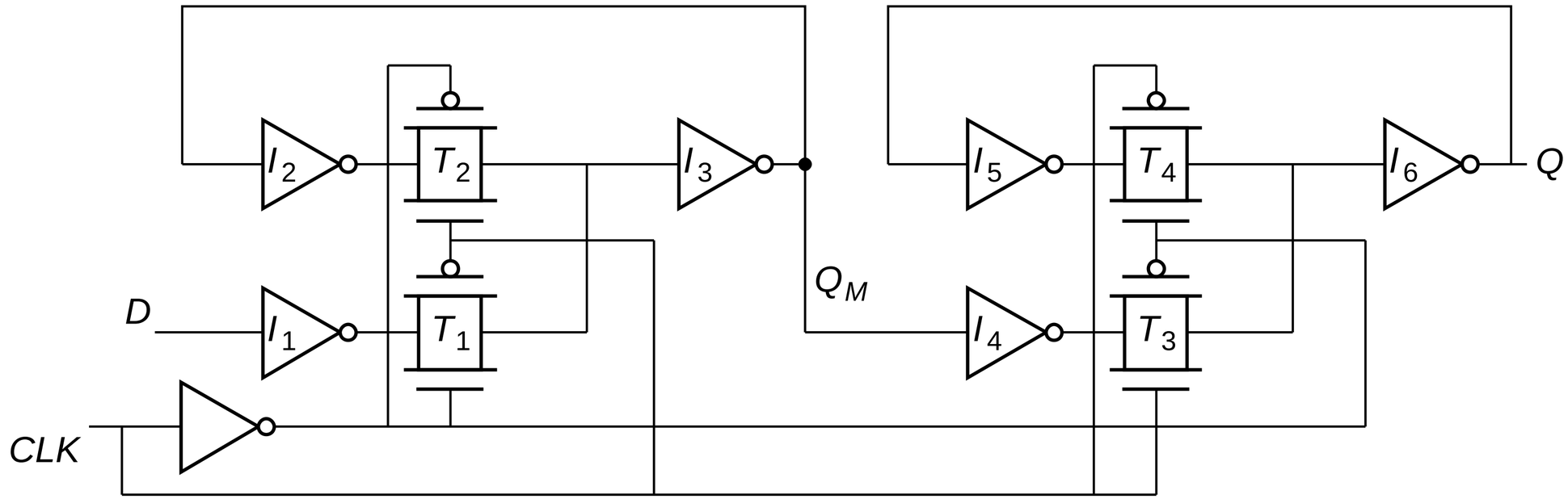
MASTER-SLAVE (EDGE-TRIGGERED) REGISTER



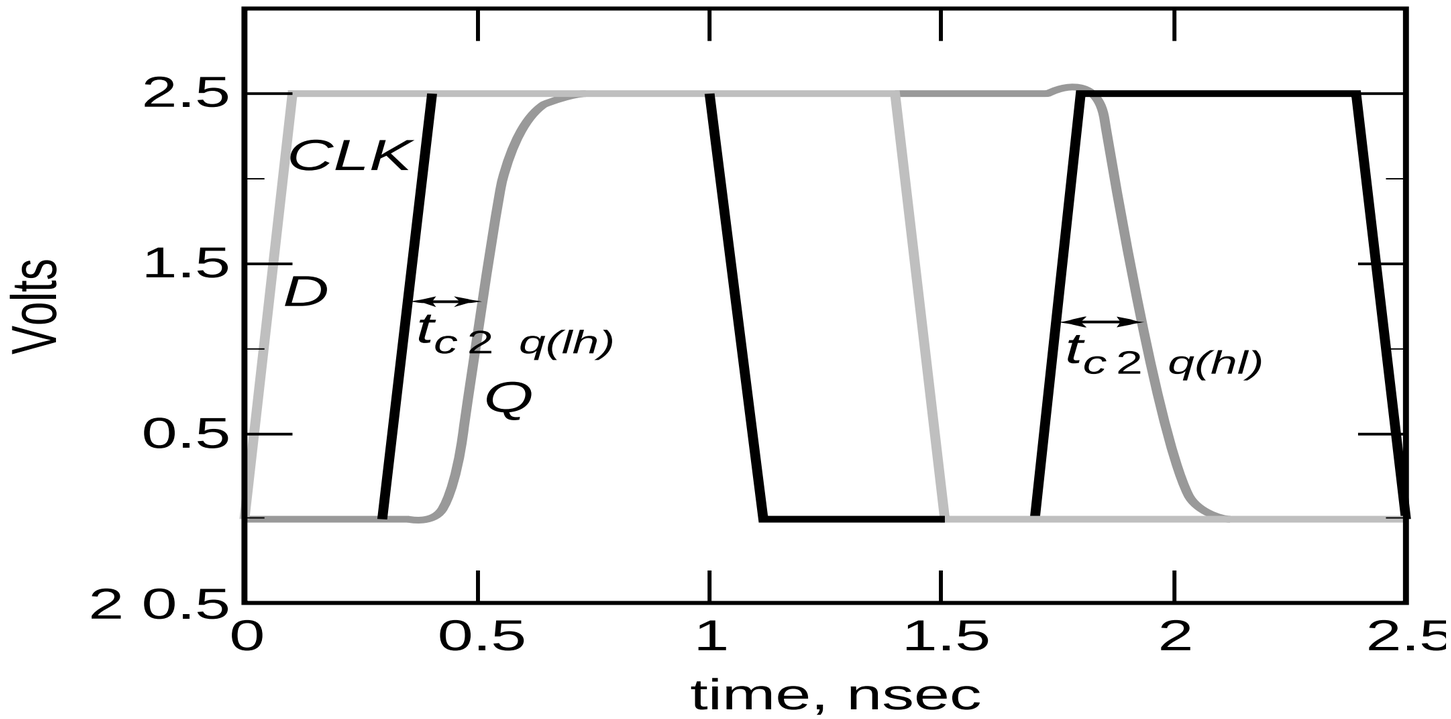
Two opposite latches trigger on edge
Also called master-slave latch pair

MASTER-SLAVE REGISTER

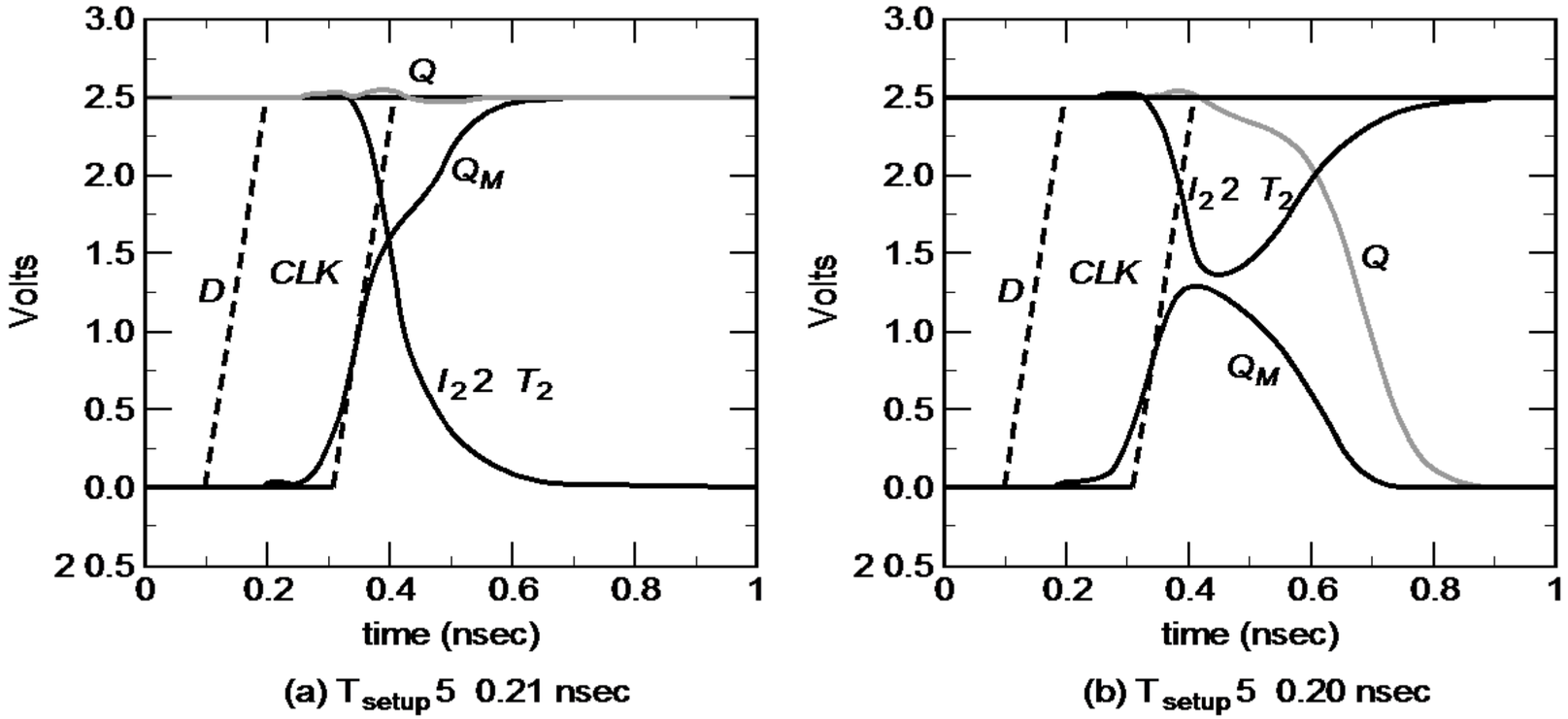
Multiplexer-based latch pair



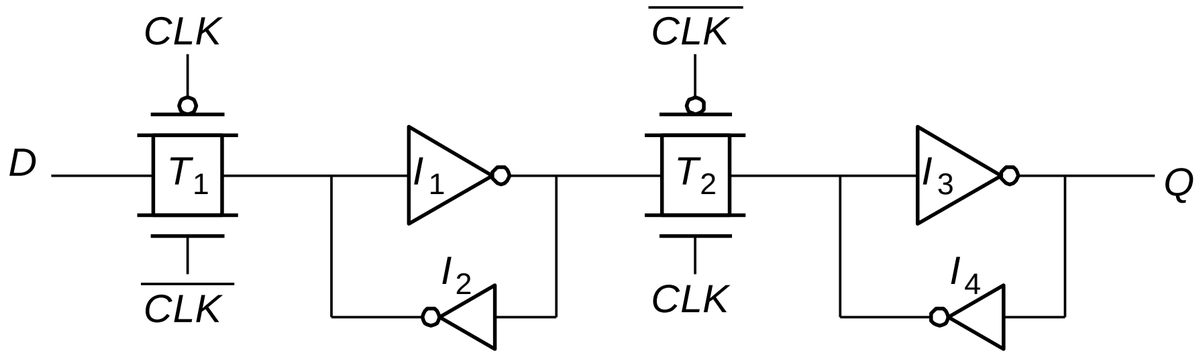
CLK-Q DELAY



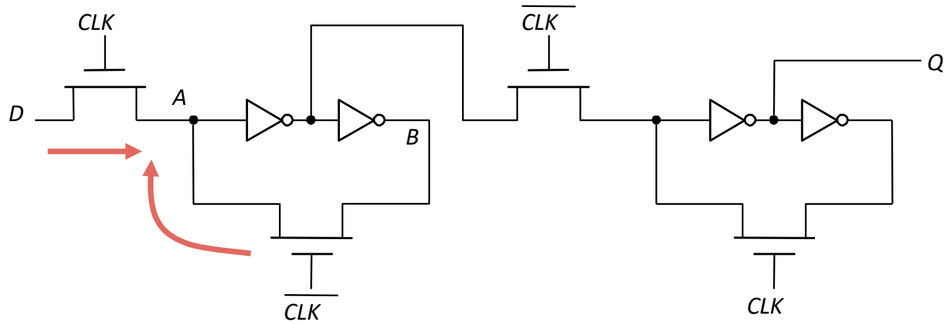
SETUP TIME


3.0
2.5
2.0
1.5
1.0
0.5
0.0
2 0.5
Volts
Q
Q_M
D
CLK
$I_2$2 T_2
0
0.2
0.4
0.6
0.8
1
time (nsec)
(a) T_{setup} 5 0.21 nsec
3.0
2.5
2.0
1.5
1.0
0.5
0.0
2 0.5
Volts
D
CLK
$I_2$2 T_2
Q
Q_M
0
0.2
0.4
0.6
0.8
1
time (nsec)
(b) T_{setup} 5 0.20 nsec

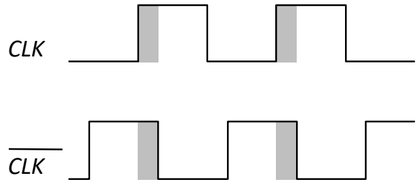
REDUCED CLOCK LOAD MASTER-SLAVE REGISTER



AVOIDING CLOCK OVERLAP

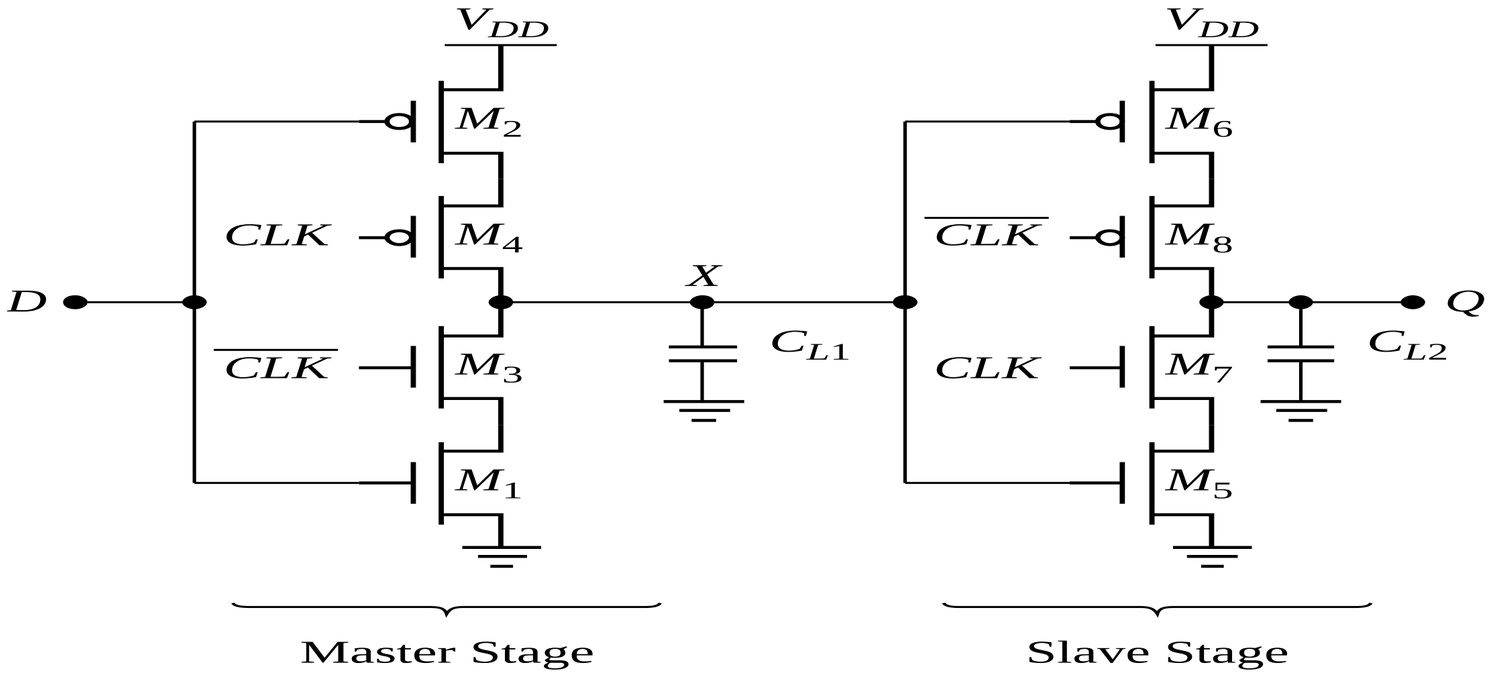


a) Schematic diagram



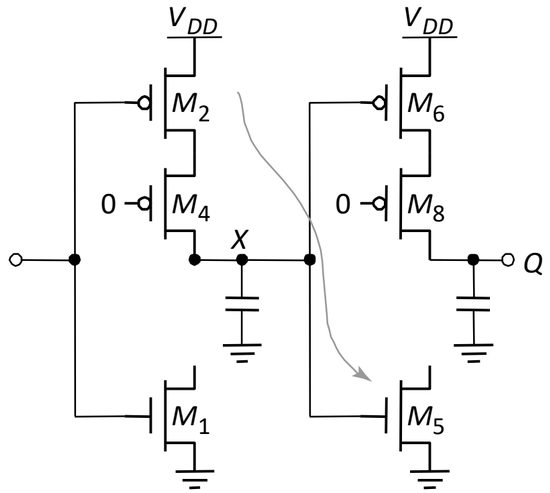
b) Overlapping clock pairs

OTHER LATCHES/REGISTERS: C²MOS

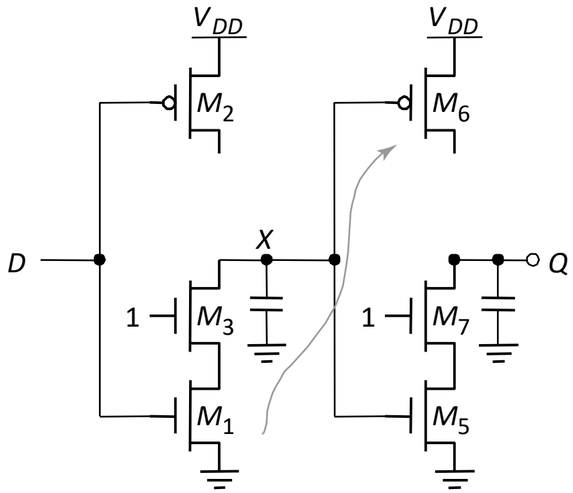


"Keepers" can be added to make circuit pseudo-static

INSENSITIVE TO CLOCK-OVERLAP

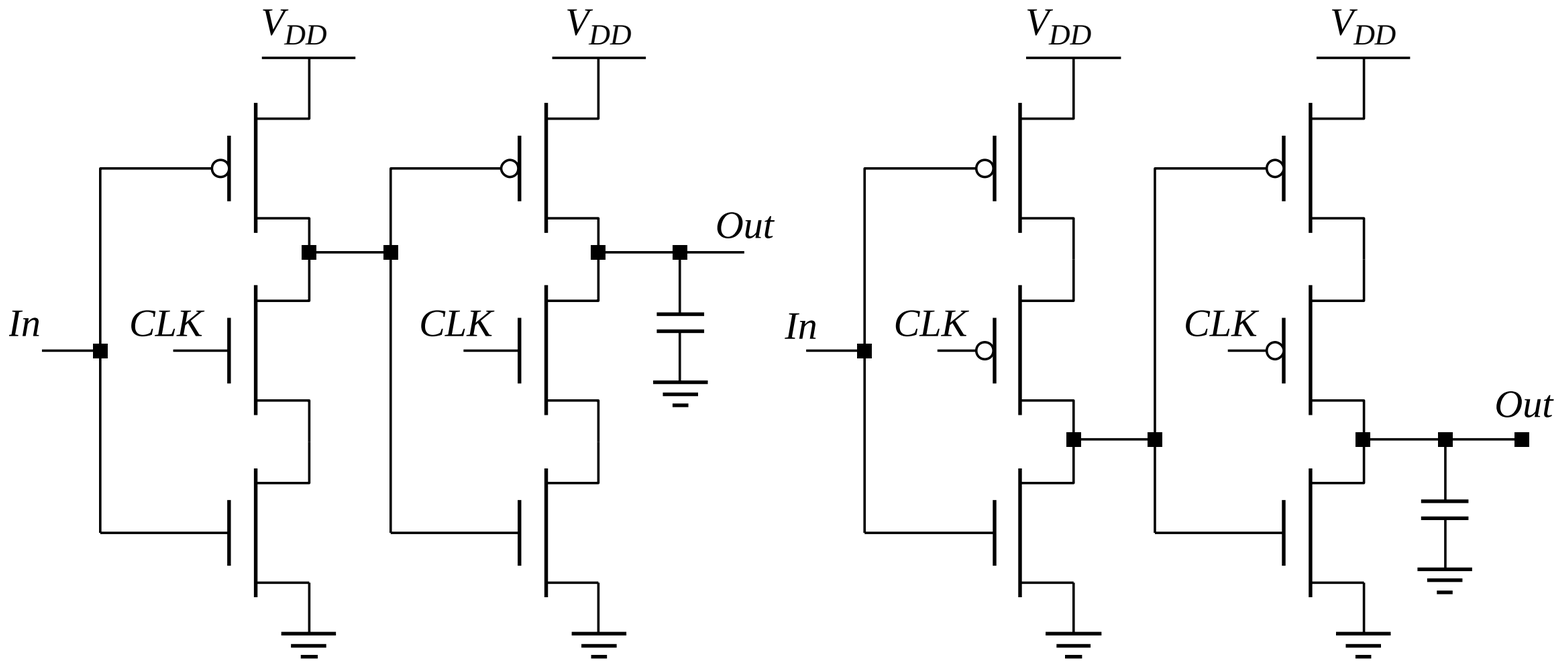


(a) (0-0) overlap



(b) (1-1) overlap

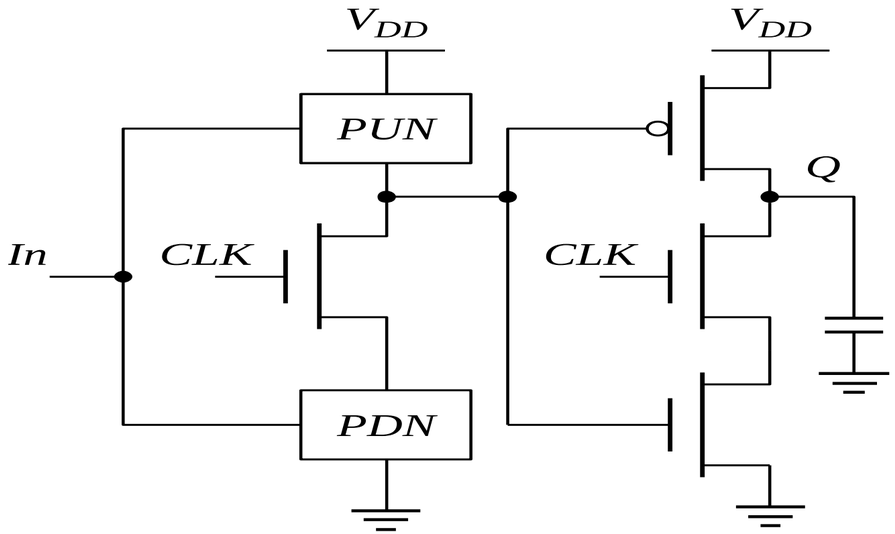
OTHER LATCHES/REGISTERS: TSPC



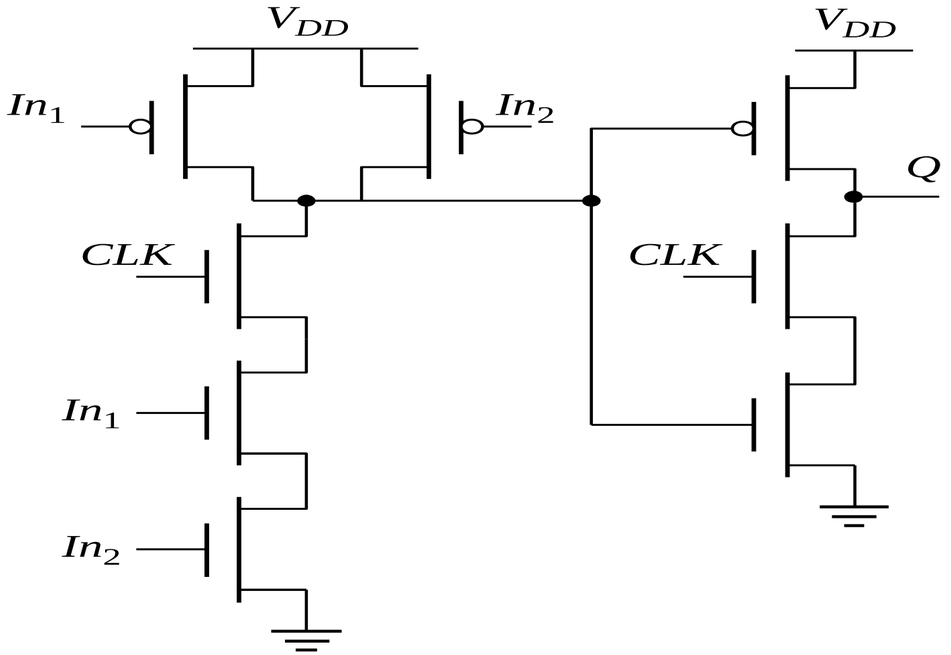
Positive latch
(transparent when CLK= 1)

Negative latch
(transparent when CLK= 0)

INCLUDING LOGIC IN TSPC

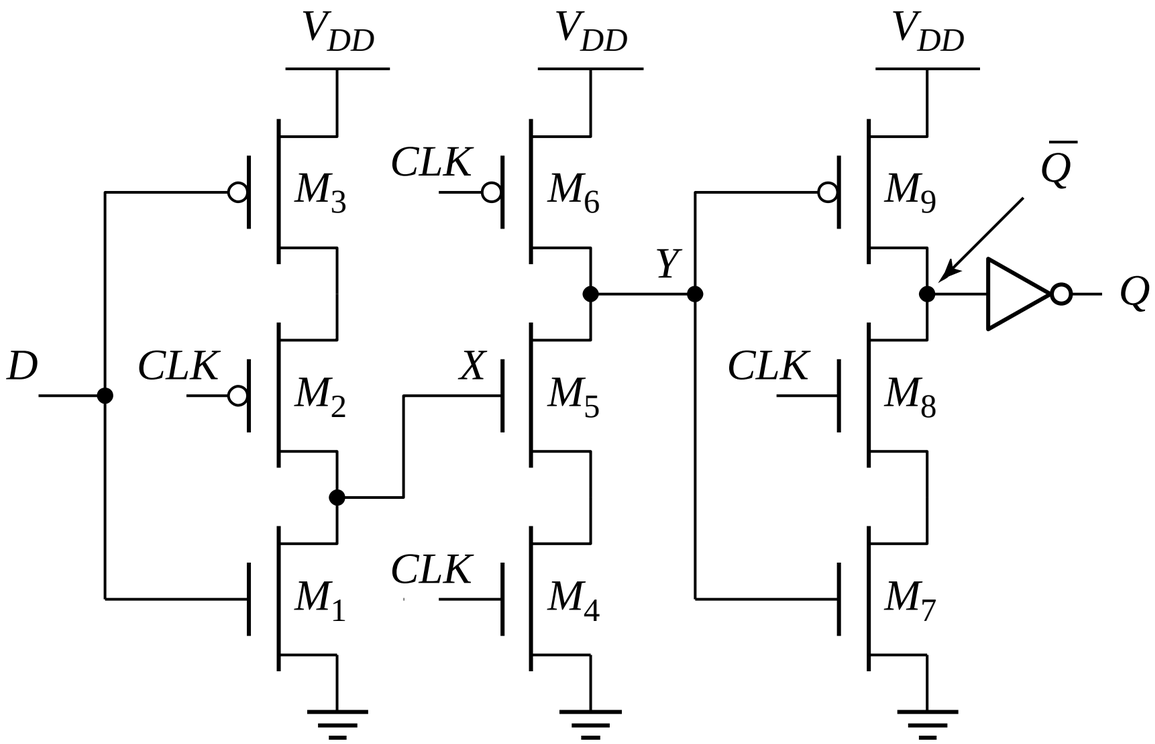


Example: logic inside the latch



AND latch

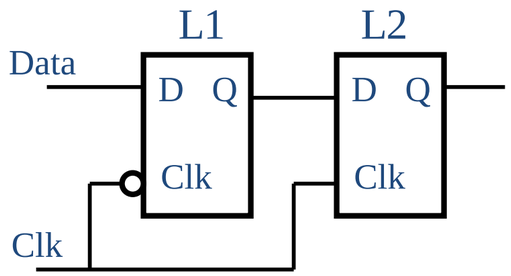
TSPC REGISTER



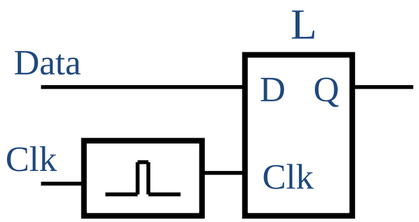
PULSE-TRIGGERED LATCHES
AN ALTERNATIVE APPROACH

Ways to design an edge-triggered sequential cell:

Master-Slave Latches



Pulse-Triggered Latch



ASSESSMENT

1. Compare Latch vs Register
2. Define Bi stability
3. Draw Master slave flip flop using latches

SUMMARY & THANK YOU