



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

16EC303–VLSI DESIGN

III YEAR/₁ V SEMESTER

UNIT 2 –COMBINATIONAL LOGIC CIRCUITS

TOPIC 5– STATIC AND DYNAMIC CMOS DESIGN



OUTLINE



- **STATIC VS DYNAMIC CMOS DESIGN**
- **COMPLEMENTARY CMOS LOGIC GATES**
- **NMOS OPERATION**
- **COMPLEX GATE**
- **DYNAMIC CIRCUIT LOGIC**
- **PRECHARGE & EVALUATE**
- **ACTIVITY**
- **COMPARISON OF CMOS CIRCUITS & EVALUATE CONTD..NMOS OPERATION**
- **ADVANTAGES**
- **DYNAMIC LOGIC PROBLEMS**
- **ASSESSMENT**
- **SUMMARY & THANK YOU**



STATIC VS DYNAMIC CMOS DESIGN

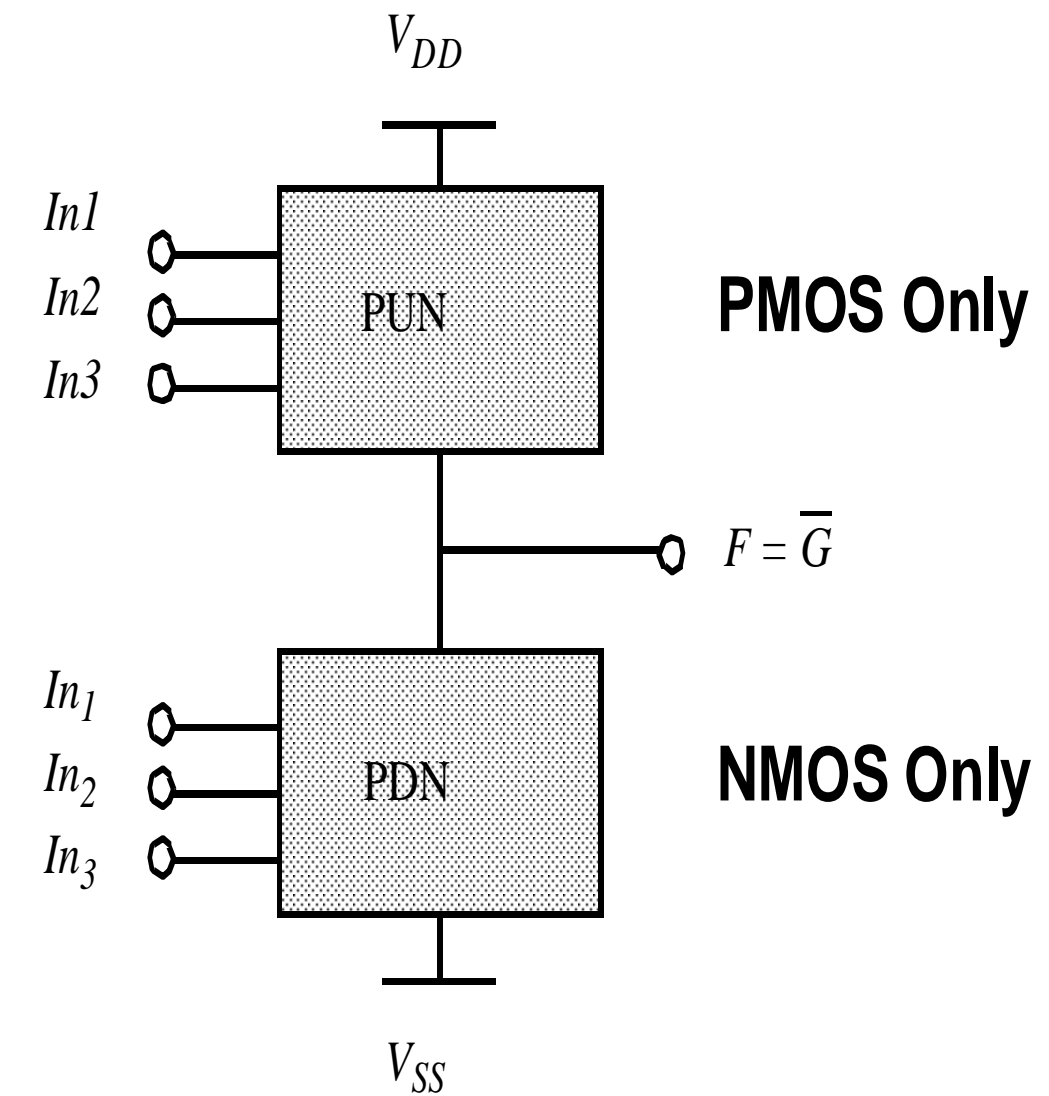


Static

Each gate output have a low resistive path to either V_{DD} or GND

Dynamic

Relies on storage of signal the value in a capacitance
requires high impedance nodes



PUN and PDN are Dual Networks

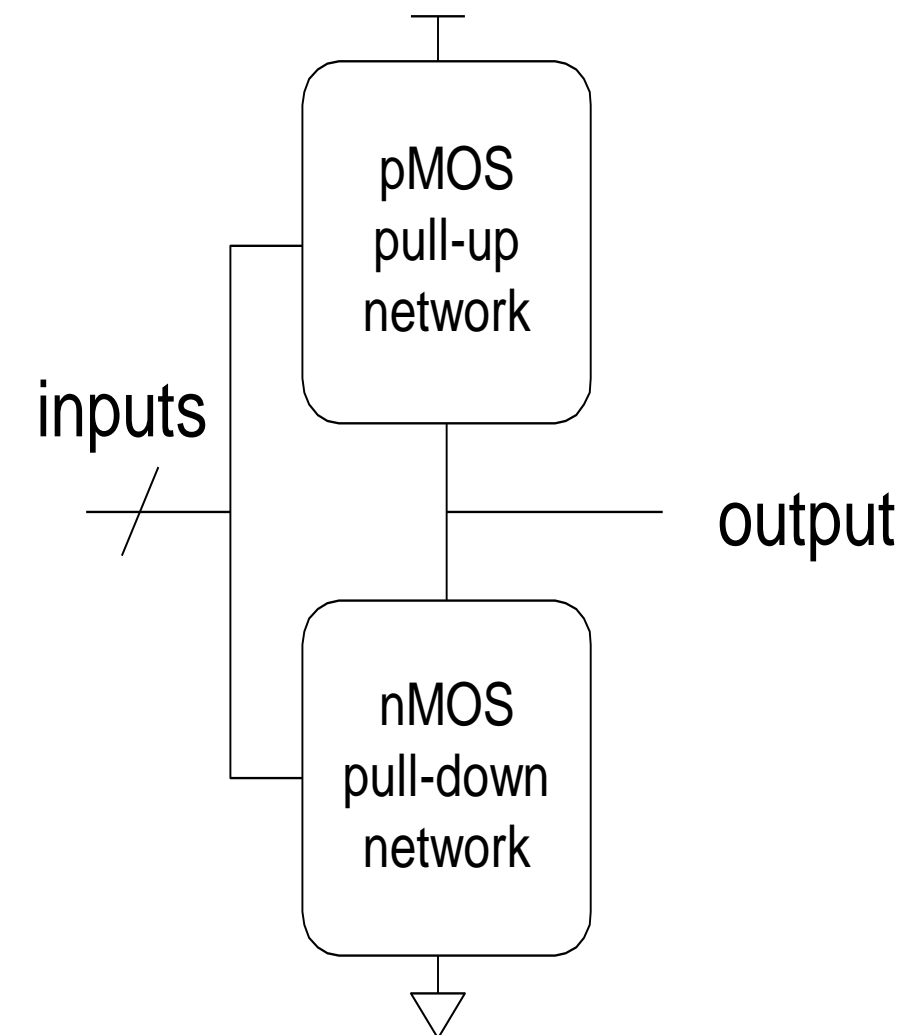


COMPLEMENTARY CMOS LOGIC GATES



- nMOS pull-down network
- pMOS pull-up network
- a.k.a. static CMOS

	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)



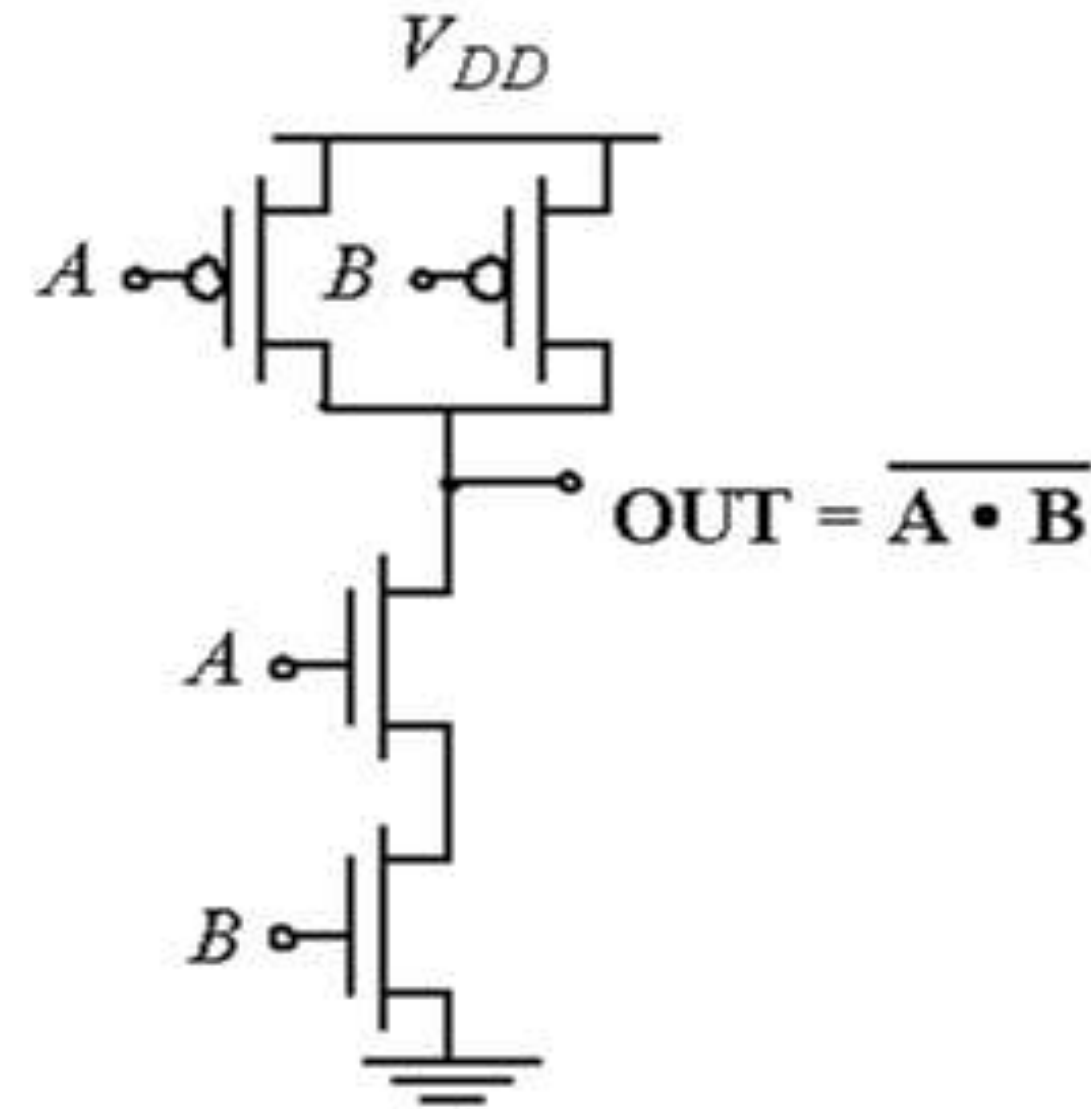


EXAMPLE GATE: NAND



A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

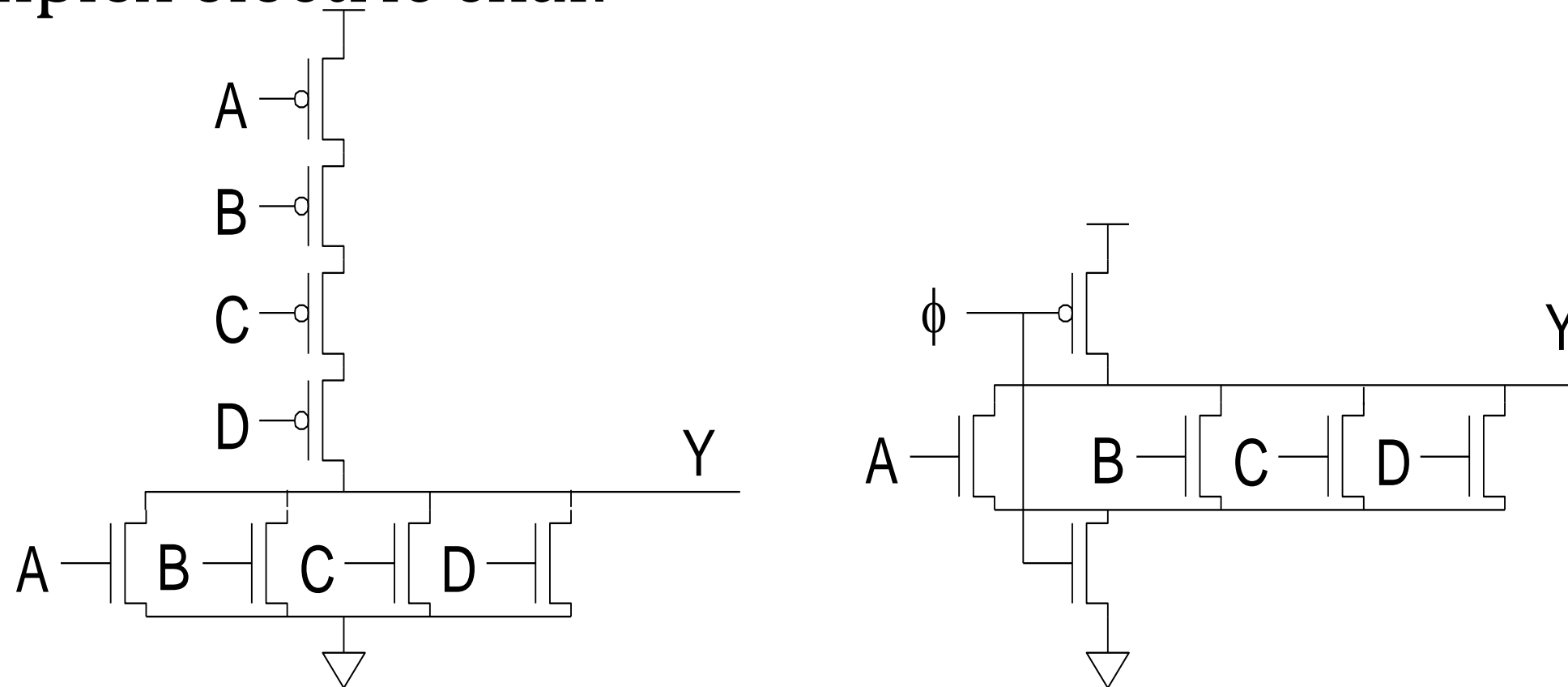




DYNAMIC C-MOS LOGIC CIRCUITS-BASIC PRINCIPLES-INTRODUCTION



- Dynamic gates use a clocked pMOS pull-up
- To design high speed cascades
- Some cascades dissipates large amt of power
- Slow pFETs eliminate, clk- used for gate, data syn.
- Complex electric char.





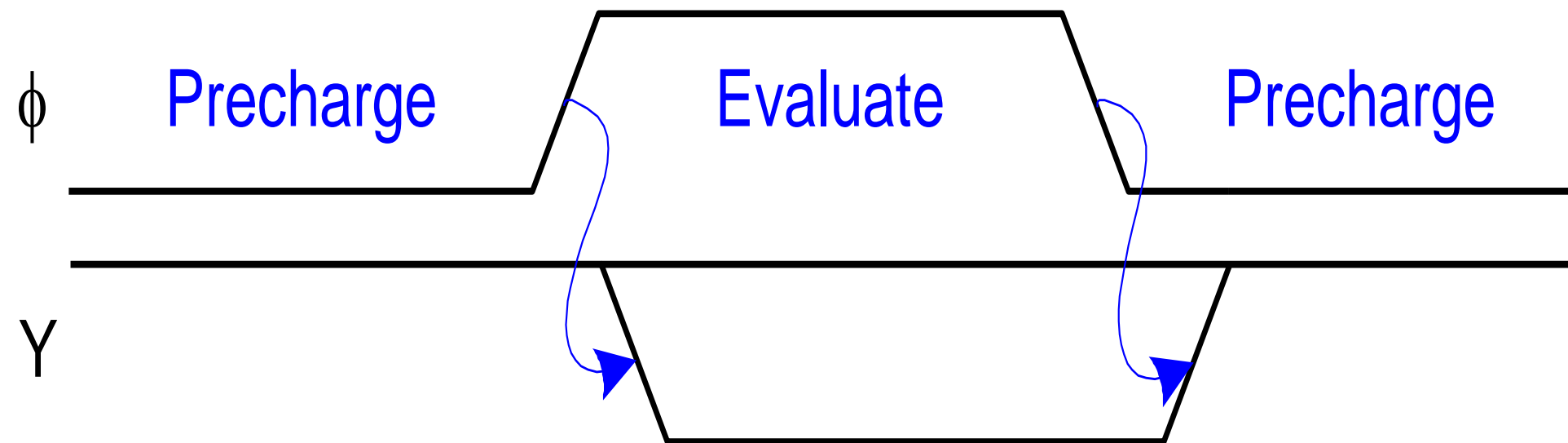
DYNAMIC CIRCUIT LOGIC

Static circuits are slow because fat pMOS load input

Dynamic gates use precharge to remove pMOS transistors from the inputs

Precharge: $f = 0$ output forced high

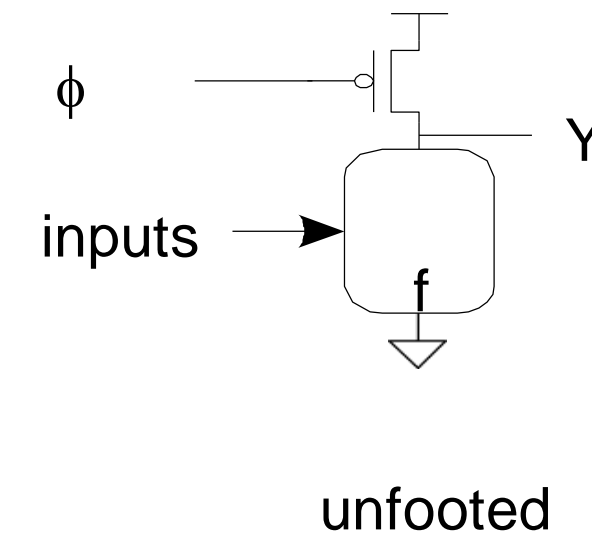
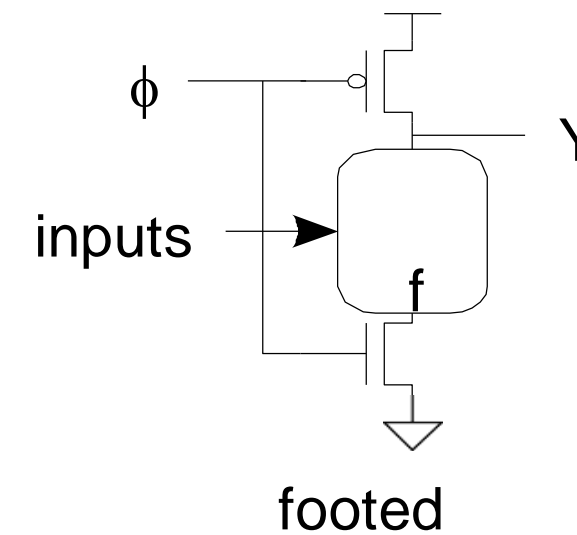
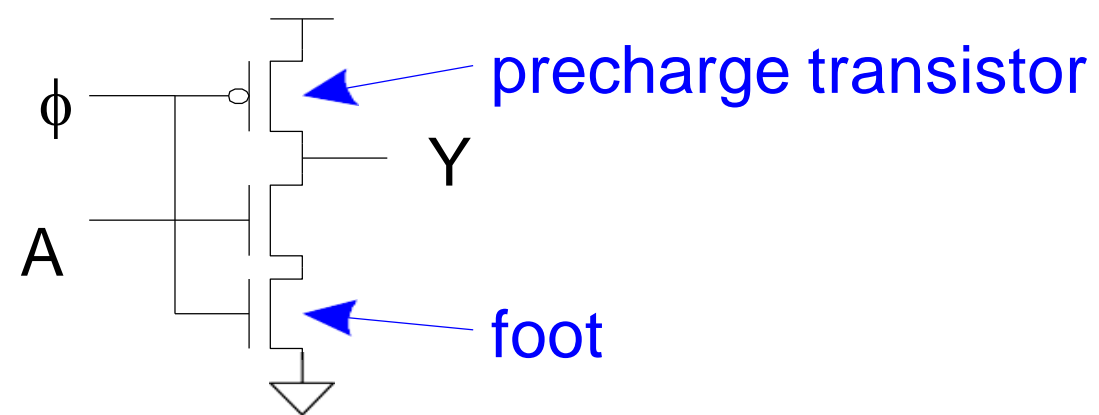
Evaluate: $f = 1$ output may pull low





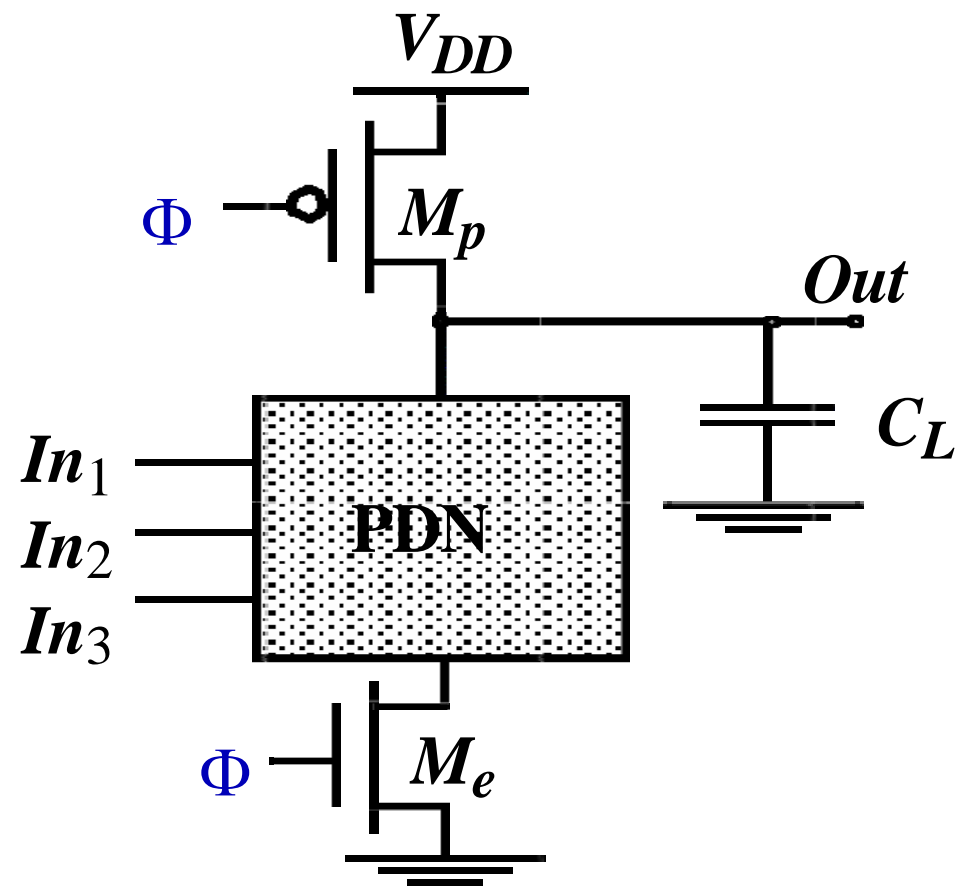
THE FOOT

- What if pulldown network is ON during precharge?
- Use series evaluation transistor to prevent fight.





DYNAMIC LOGIC: PRINCIPLES



- **Precharge:** $\Phi = 0$, *Out* is precharged to V_{DD} by M_p . M_e is turned off, no dc current flows (regardless of input values)
- **Evaluation**
 $\Phi = 1$, M_e is turned on, M_p is turned off. Output is pulled down to zero depending on the values on the inputs. If not, precharged value remains on C_L .

Important: Once *Out* is discharged, it cannot be charged again! Gate input can make only one transition during evaluation

- Minimum clock frequency must be maintained
- Can M_e be eliminated?



PRECHARGE & EVALUATE

It uses single clk ctrl comple.pair-Mp,Mn

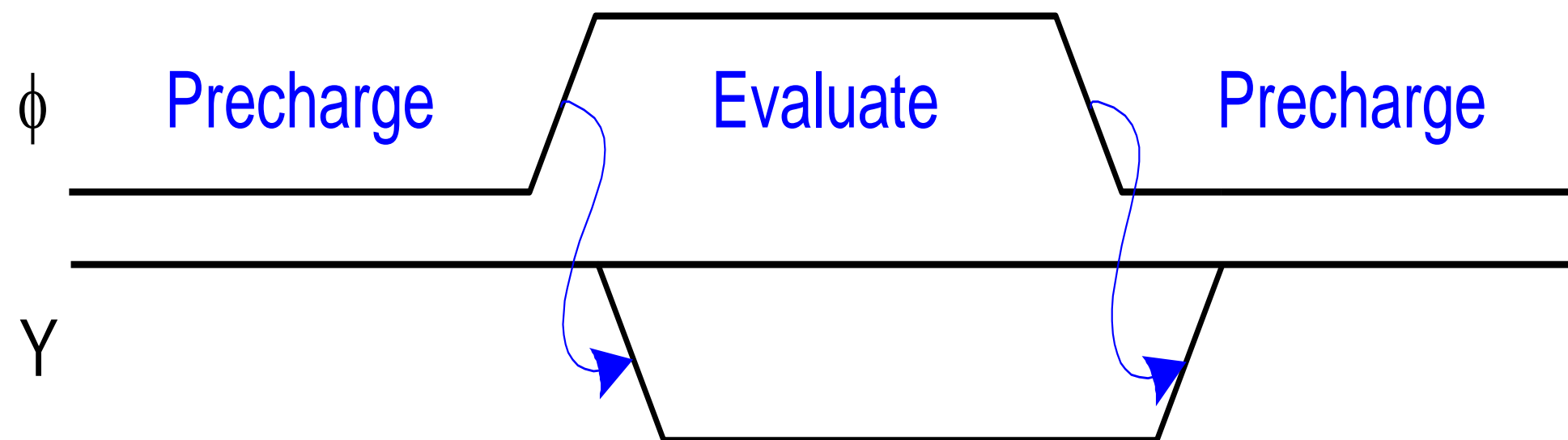
Array of nFET-open or closed switch dep. on i/p(any one FET enough for 'sw')
oper. ctrl by clk

Clk=0 → **precharge** Mp-ON,Mn-OFF

Cout to charge to value $V_{out}=V_{dd}$,every half cycle

Clk=1 → **evaluate** of the operational cycle

Mp-OFF,Mn-ON.a,b,c accept into nFET logic array





ACTIVITY

BRAIN TEASER



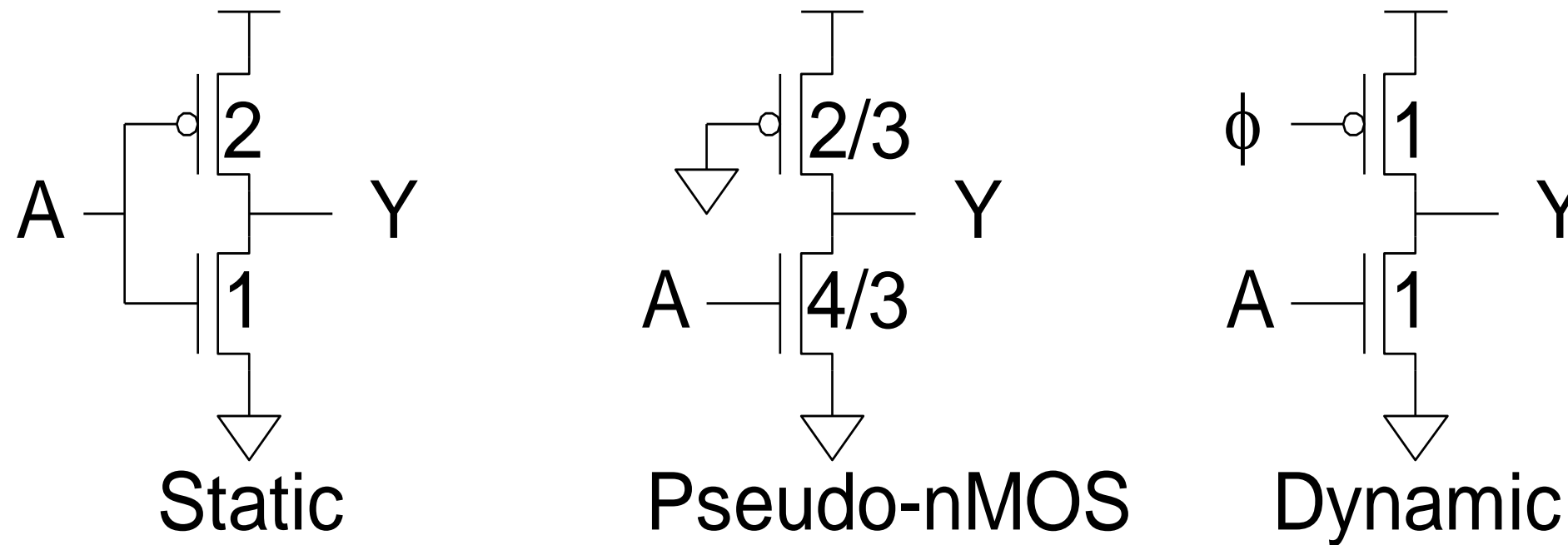
Look at this series:

7, 10, 8, 11, 9, 12, ...

What number should come
next?



COMPARISON OF CMOS CIRCUITS & EVALUATE CONTD..



If array acts open sw \rightarrow V_{out} held at $V_{dd} = f=1$.

If closed sw \rightarrow $C_{out} - V_{out} = 0v$, so $f=0$

*the sequence occurs every clk cycle

Ex:

DYNAMIC NOR2, NAND2 GATES



DYNAMIC LOGIC ADVANTAGES



- To design high speed cascades
- Some cascades dissipates large amt of power
- Slow pFETs eliminate, clk- used for gate, data syn.
- Complex electric char.
- $N+2$ transistors for N -input function
 - Better than $2N$ transistors for complementary static CMOS
 - Comparable to $N+1$ for ratio-ed logic
- No static power dissipation
 - Better than ratio-ed logic
- Careful design, clock signal needed



DYNAMIC LOGIC PROBLEMS

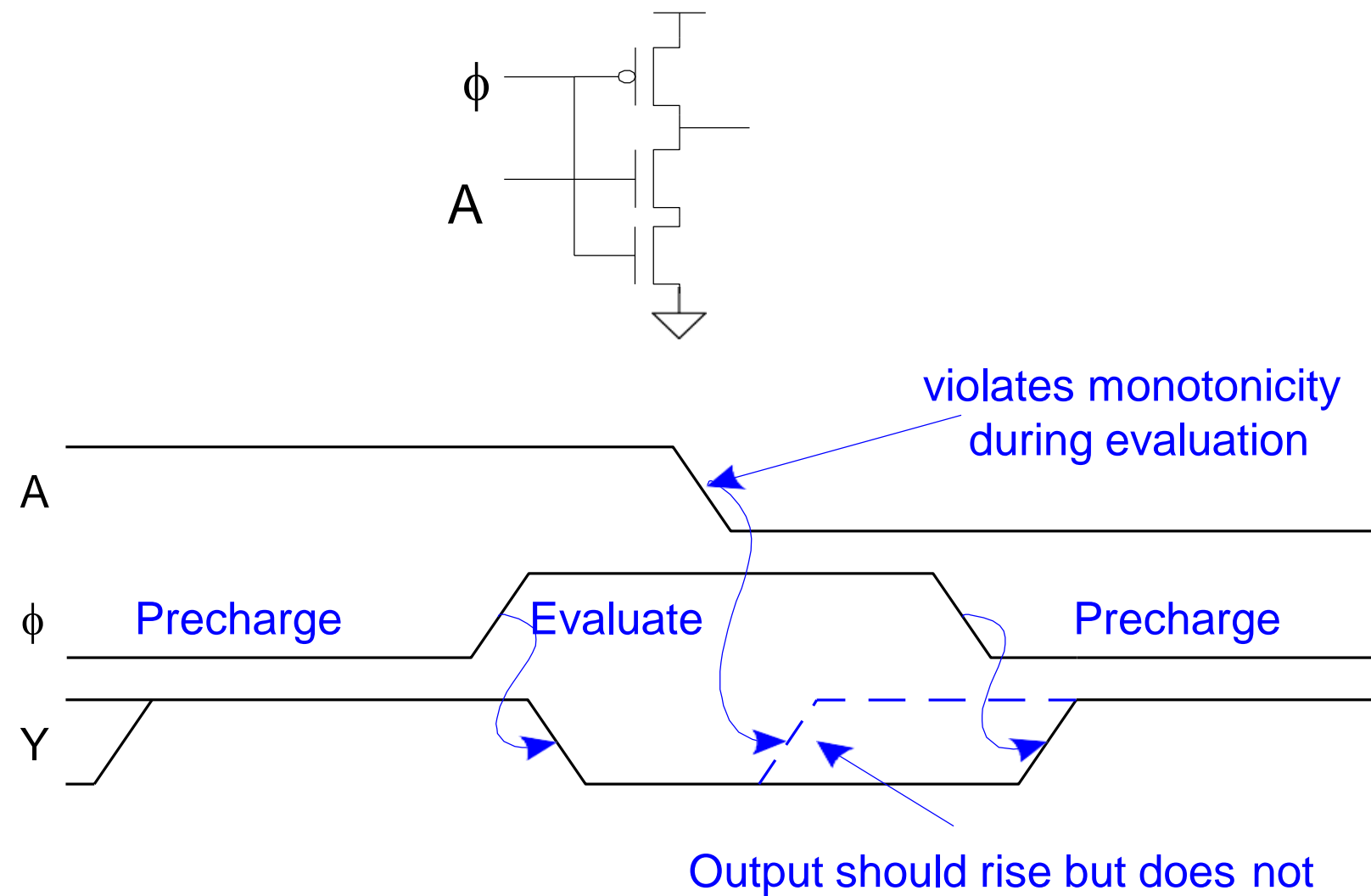


- Monotonicity
- Charge Leakage
- Charge Sharing
- Capacitive Coupling
- Clock Feed through



MONOTONICITY

- Dynamic gates require monotonically rising inputs during evaluation
 - 0 -> 0
 - 0 -> 1
 - 1 -> 1
 - But not 1 -> 0

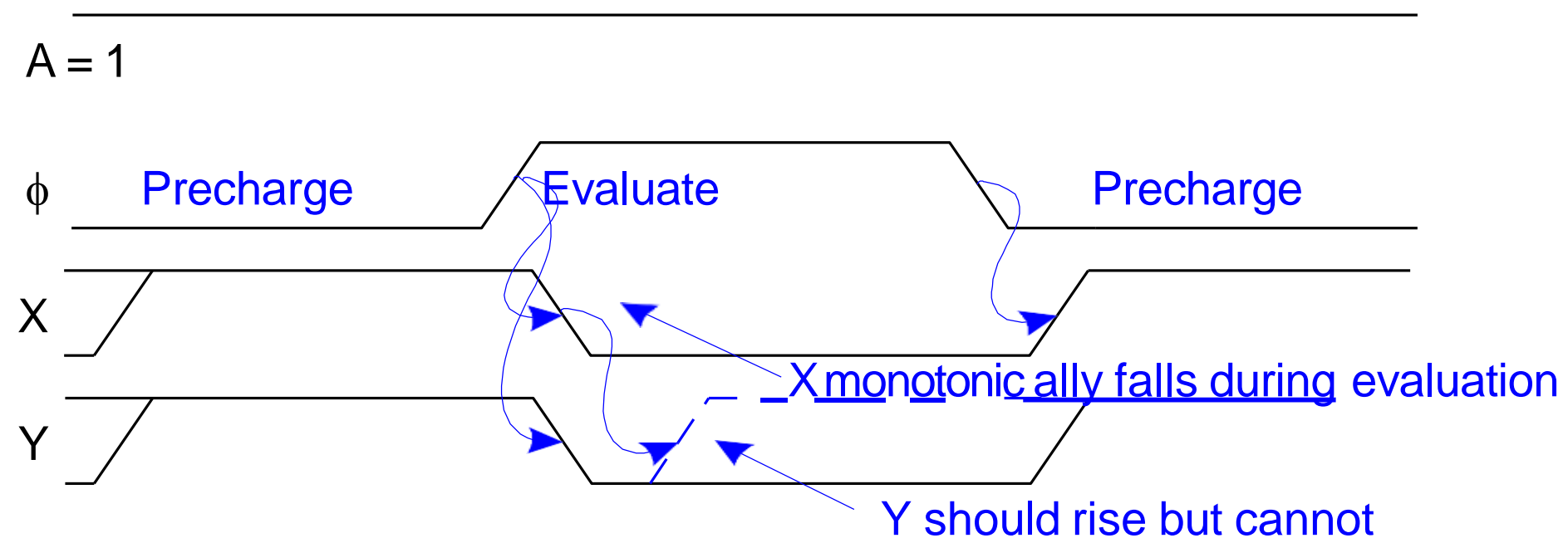
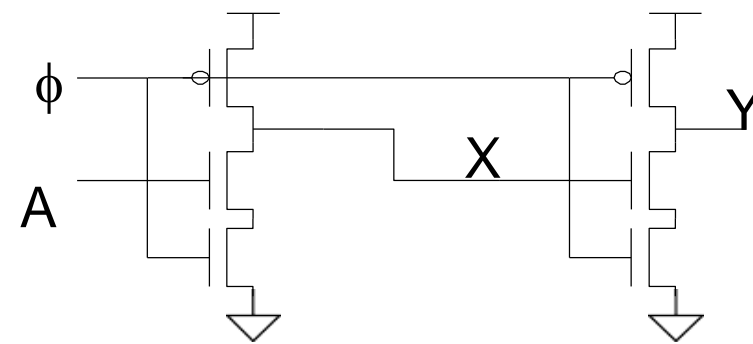




MONOTONICITY WOES



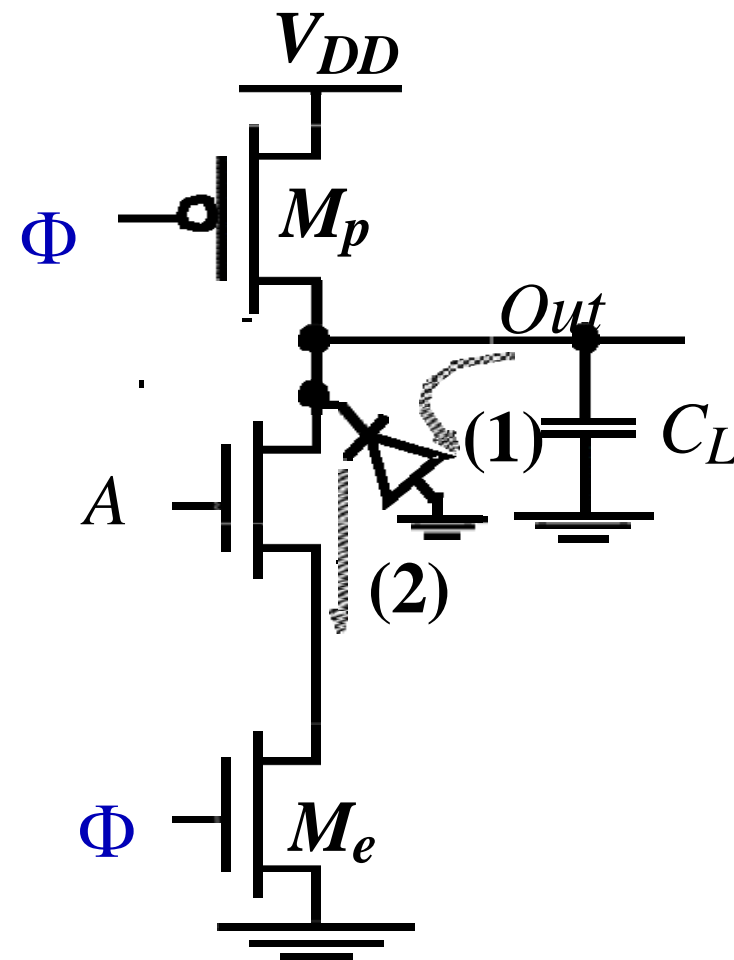
- But dynamic gates produce monotonically falling outputs during evaluation
- Illegal for one dynamic gate to drive another!



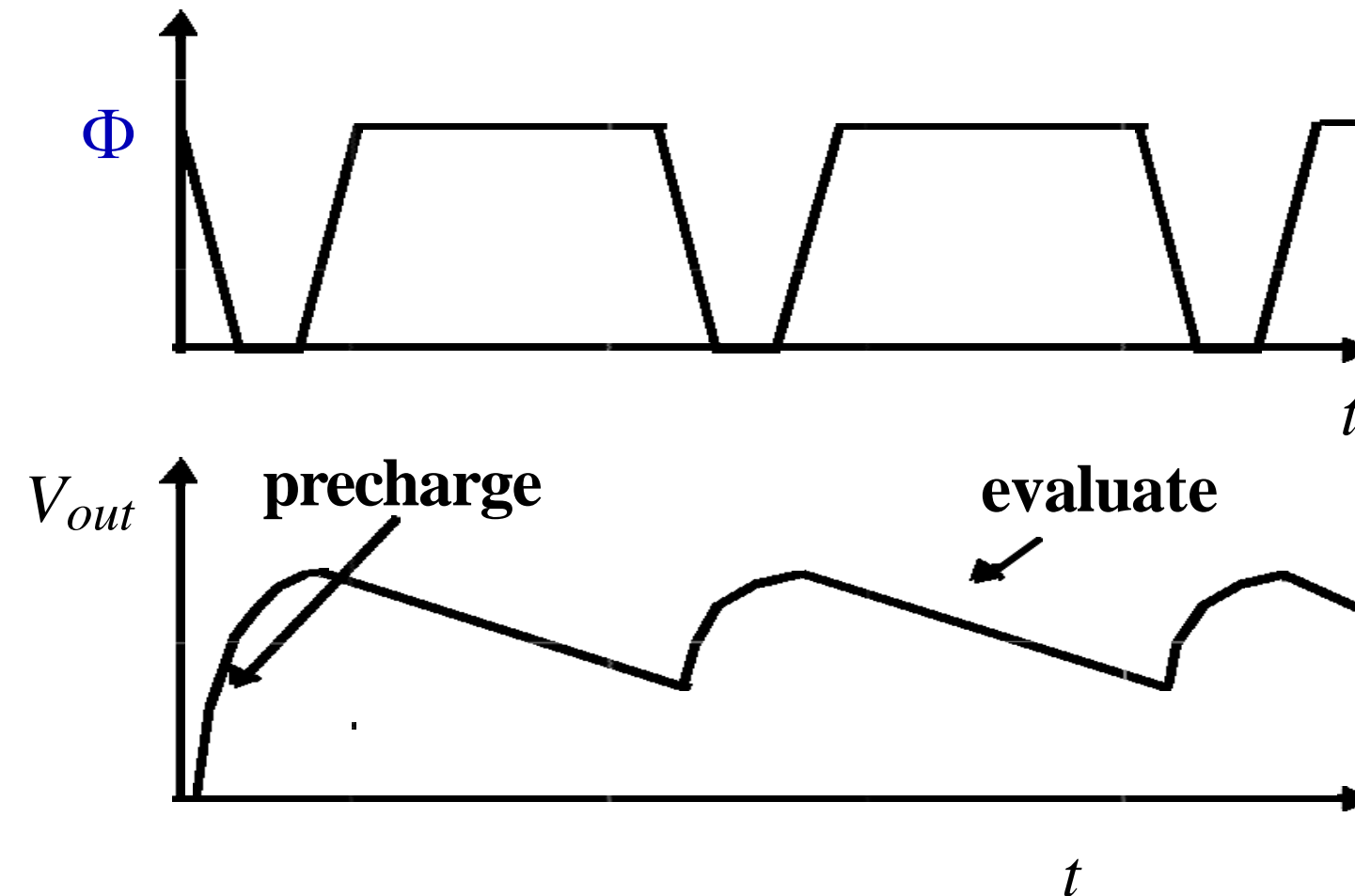
James Morizio



RELIABILITY PROBLEMS — CHARGE LEAKAGE



(a) Leakage sources



(b) Effect on waveforms

$A = 0$

- (1) Leakage through reverse-biased diode of the diffusion area
- (2) Subthreshold current from drain to source

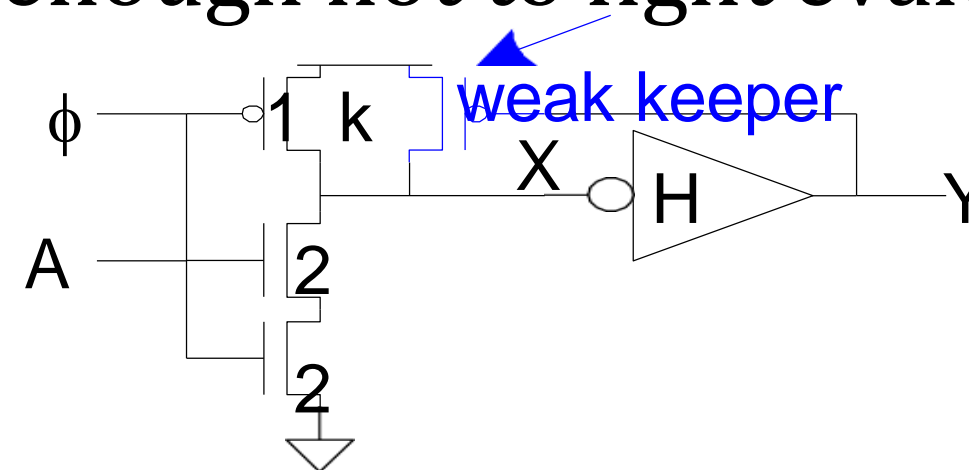
Minimum Clock Frequency: > 1 MHz



LEAKAGE

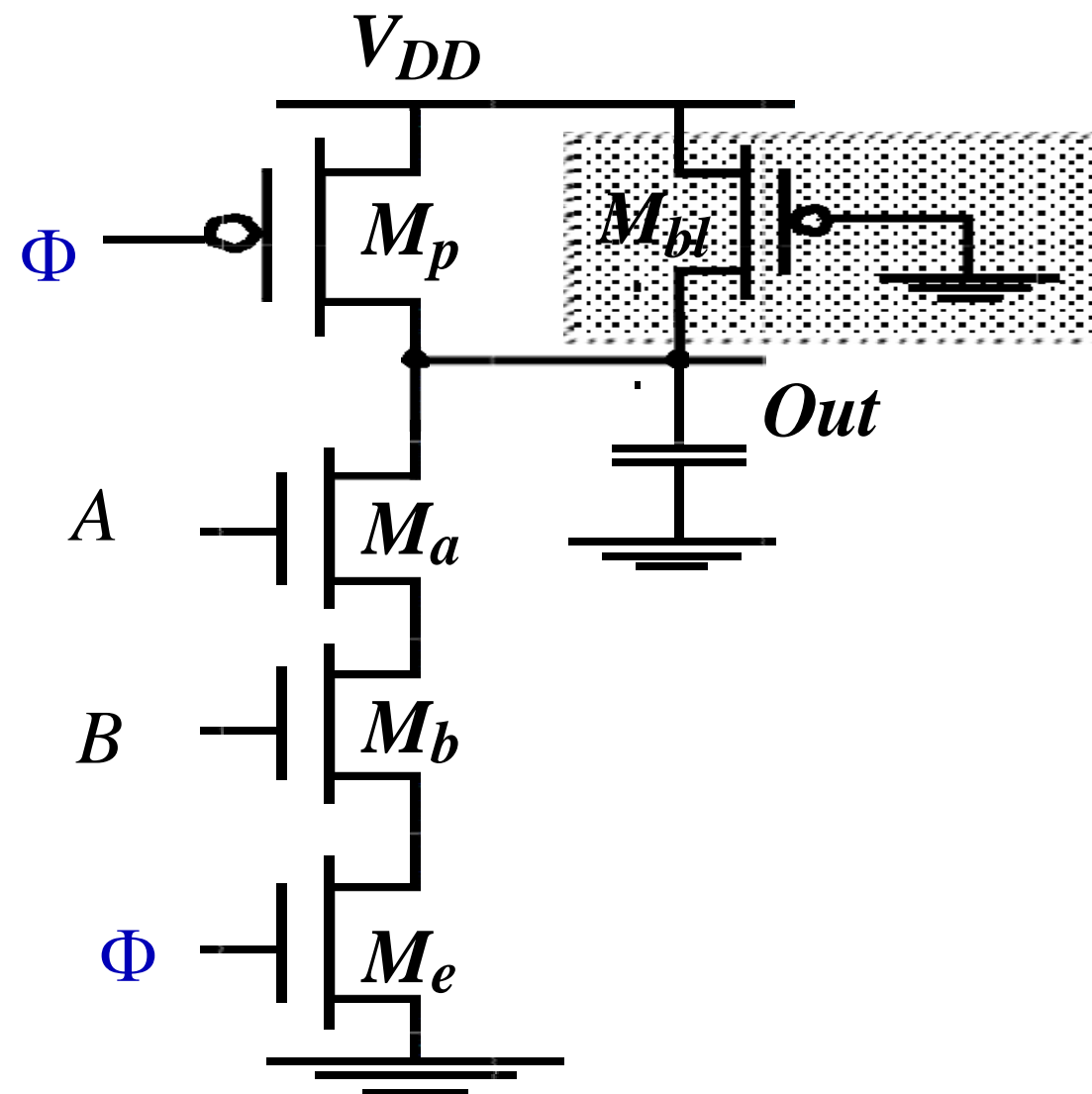


- Dynamic node floats high during evaluation
 - Transistors are leaky ($I_{OFF} \neq 0$)
 - Dynamic value will leak away over time
 - Formerly miliseconds, now nanoseconds!
- Use keeper to hold dynamic node
 - Must be weak enough not to fight evaluation

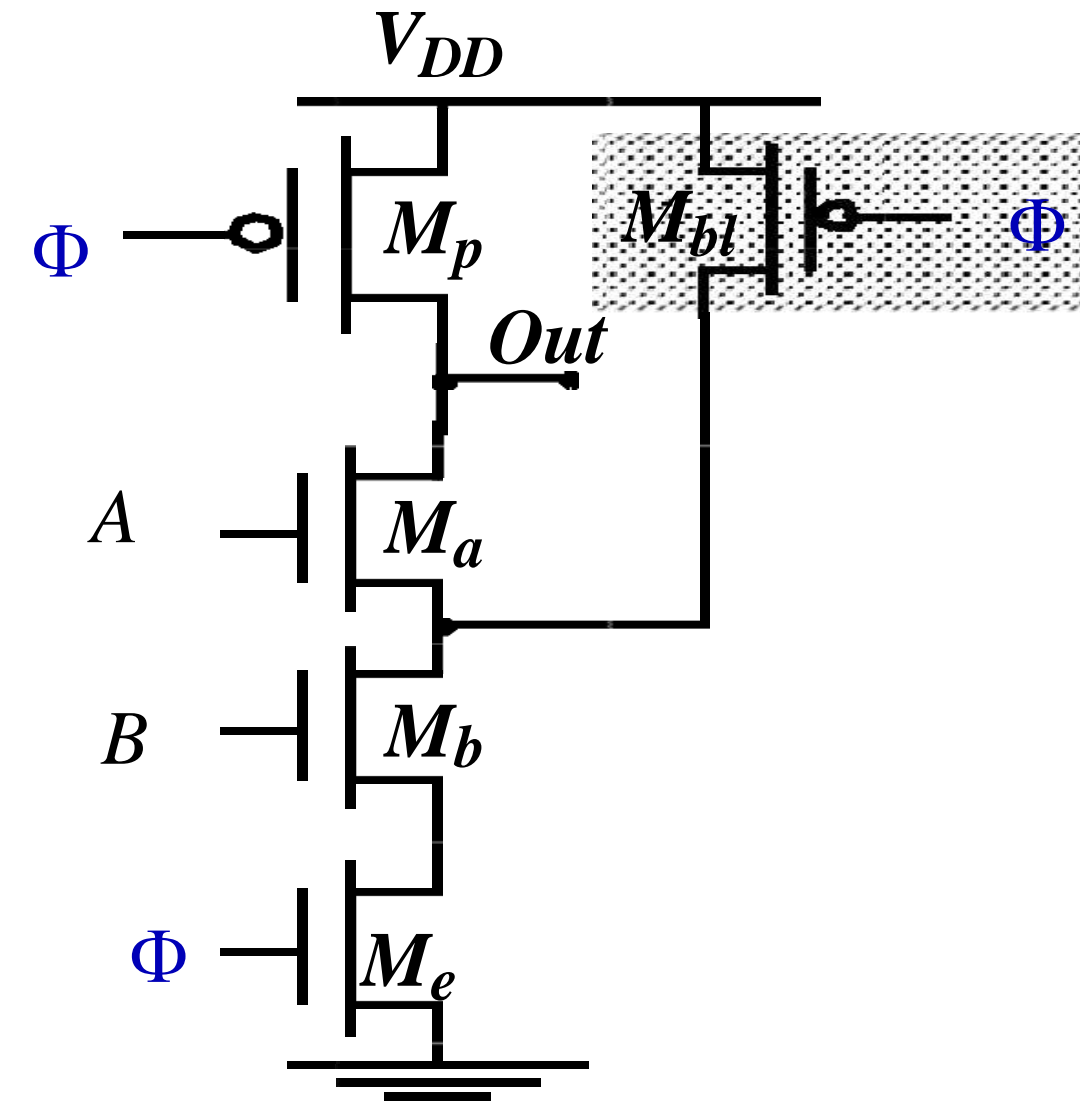




CHARGE REDISTRIBUTION - SOLUTIONS



(a) Static bleeder



(b) Precharge of internal nodes



ASSESSMENT



- Compare Static & Dynamic logic
- List out dynamic logic problems
- How monotonicity problem is solved?



SUMMARY & THANK YOU