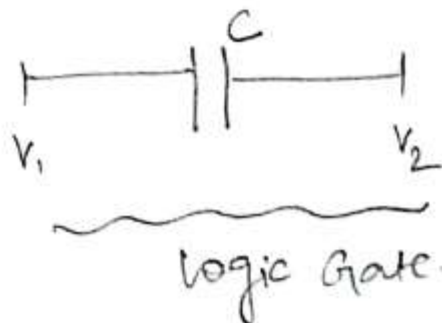
MOS transistor - C-V characteristics.

→ Capacitances are Non Linear and voltage dependent (C-V).

→ Simple capacitors approximated, when its behaviour is averaged across switching voltages of a logic gate.



$$\frac{V_1 + V_2}{2} = \text{'C' behaviour}$$

→ To estimate delay and Power consumption of transistors.

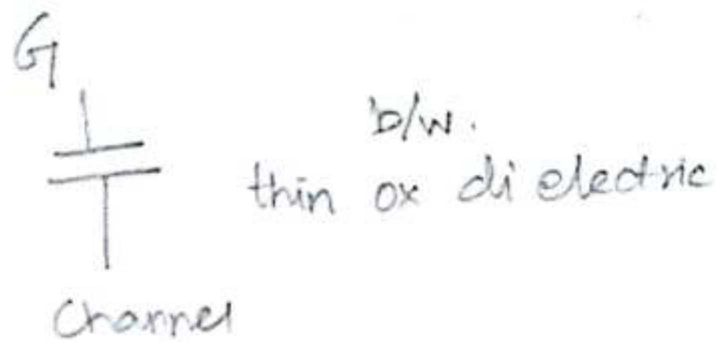
1* Simple MOS Capacitance Models.
2* Detailed MOS Gate Capacitance Model
3* Detailed MOS diffusion Capacitance Model.

1*

↳ MOS - G ⇒ good capacitor.

↳ To attract charge to invert channel Hi capacitance needed to get hi I_{ds}.

Scanned by CamScanner



So, $C_g = C_{ox} WL$ —①

* Capacitor is a 2 terminal device.
* When transistor ON → channel extends from Source & reach Drain ⓢ→ⓓ
↳ in sat.
or stops short in 'sat'.
* Most transistor used min. Manufacturable 'L'.
great speed & low power consume.

$$C_g = C_{perµ} \cdot W \quad —②$$

$$C_{perµ} = C_{ox} \cdot L = \frac{\epsilon_{ox}}{t_{ox}} \cdot L \quad —③$$

* C_G, C_D, C_S → make impact ckt. performance
so It is called "Parasitic capacitors"

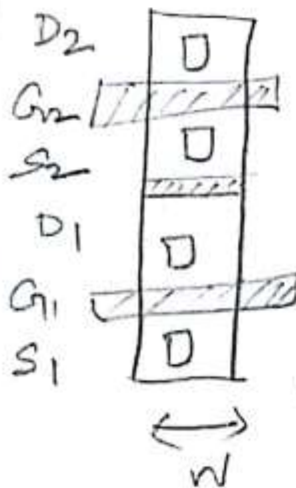
* It arises from reverse biased P-n Jn. b/w ⓢ/ⓓ diffusion & body/substrate(b)
It is called 'diffusion capacitances"
$C_{sb} \cdot C_{db}$

Scanned by CamScanner

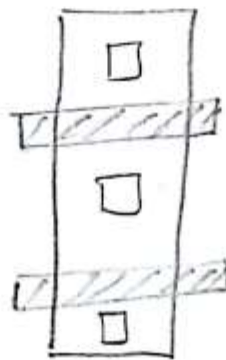
C - V ....

The size of these jn. depends on Area, and perimeter of Ⓢ, Ⓓ diffusion, depth of diffusion, doping levels & Ⓥ. So, diffusion has High C & R

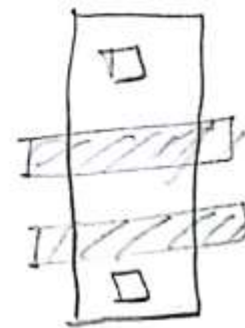
Diffusion region geometrics:



isolated



Shared



merged

2* Detailed MOS Gate Capacitance Model.

MOS gate sits above channel & partial overlap Ⓢ & Ⓓ.

a) Intrinsic capacitance (over the channel)

b) Overlap capacitance (Ⓢ, Ⓓ, Ⓑ).

$C_0 = W L C_{ox}$.

Scanned by CamScanner

Cutoff :-

When transistor is off ($V_{gs}=0$) channel is not inverted and charge on gate is matched with opposite charge from body.

C_{gb} → gate to body capacitance.

$V_{gs} < V_t$ → depletion forms at surface. bottom plate moves downward from ox reducing capacitance.

Linear.

$V_{gs} > V_t$ channel inverts and again serves good conductive bottom plate. However ch- is connected to Ⓢ & Ⓓ rather than Ⓑ. * At low V_{ds} the channel charge shared b/w Ⓢ $\frac{}{q}$ Ⓓ

$$C_{gs} = C_{gd} = C_0/2$$

* As V_{ds} increases the region near Ⓓ less inverted, so greater fraction of c' attributed to Ⓢ & small fraction to Ⓓ.

Sat :-

$V_{ds} > V_{gs} - V_t$ channel- pinched off

All intrinsic c' is to Ⓢ.

$$\boxed{C_{gs} = 2/3\, C_0}$$

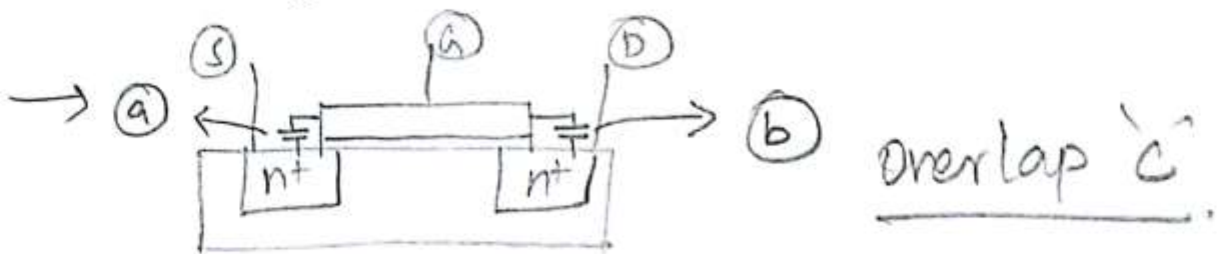
Scanned by CamScanner

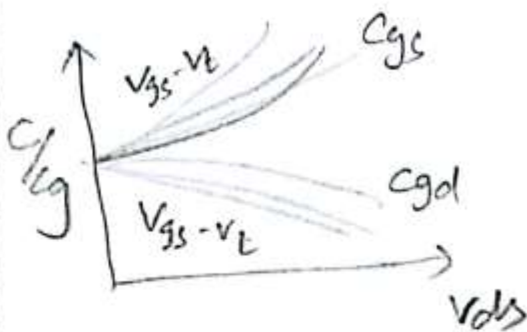
	cutoff	Linear	Sat
C_{gb}	C_o	0	0
C_{gs}	0	$C_o/2$	$\frac{2}{3} C_o$
C_{gd}	0	$C_o/2$	0
$C_g = C_{gb} + C_{gs} + C_{gd}$	C_o	C_o	$\frac{2}{3} C_o$.

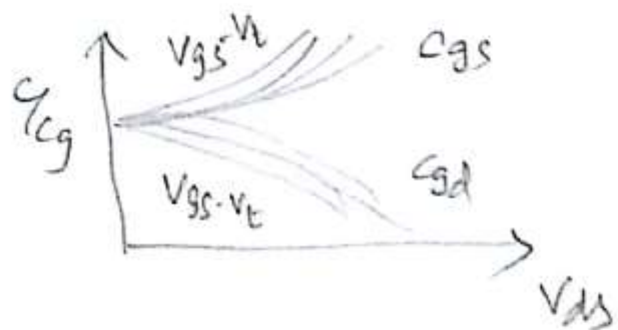
$$C_g = C_{gb} + C_{gs} + C_{gd} \sim C_o$$

→ (a) C_{gs} (overlap) $= C_{gsol} \cdot W$

(b) C_{gd} (overlap) $= C_{gdol} \cdot W$.







⇓

C → vary as a fn. of V_{ds} for no. of $V_{gs}-V_t$

⇓

Short-ch-transisi

$C_{gd} \neq 0$ → sat

C_g → charge based model

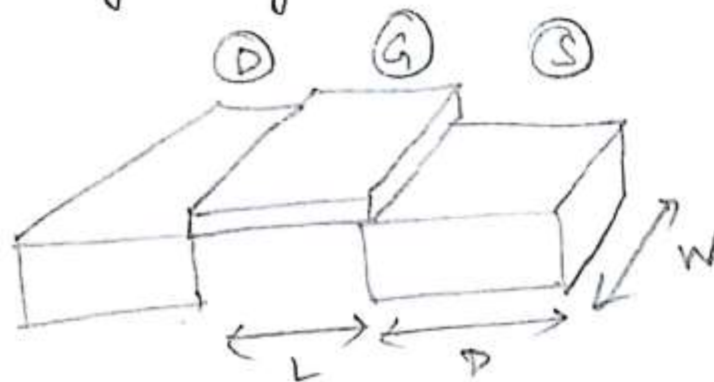
C_{gd} (overlap) → signifi- - Cant

Coverlap → voltage dependence. for delay cal.

Scanned by CamScanner

3* Detailed MOS diffusion capacitance Model.

Diffusion region geometry.



$AS = W \cdot D$ $\quad PS = 2W + 2D$

Total source parasitic 'C'.

$$C_{sb} = AS \cdot C_{jbs} + PS \cdot C_{jbssw} \quad \text{--- (1)}$$

↓ ⇐ unit ⟹ ↓

C/Area C/Length

* depletion region thickness dep. reverse bias.
So It's non linear.

$$C_{jbs} = C_J \left(1 + \frac{V_{sb}}{\varphi_0}\right)^{-M_J}$$

C_J → Jn. capacitance at zero bias & high process dependent.

M_J → Junction grading coefficient.

= 0.5 – 0.33.

φ_0 → built in Potential dep. on doping level.

Scanned by CamScanner

$$\psi_0 = V_T \ln \frac{N_A \cdot N_D}{n_i^2}$$

V_T → thermal voltage from thermo dynamics

Side wall Capacitance.

$$C_{jbssw} = C_{JSW}\left(1 + \frac{V_{sb}}{\psi_0}\right)^{-M_{JSSW}}$$

$$C_{jbsswg} = C_{JSWG}\left(1 + \frac{V_{sb}}{\psi_0}\right)^{-MJSWG}$$

Drain diffusion has III^r parasitic 'C' dep. on AD, PD & V_{db}.

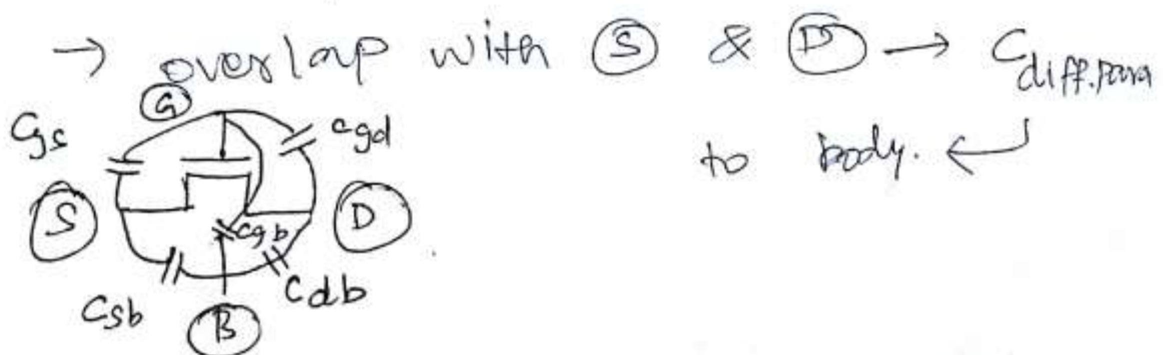
Value averaged across switching transition.

Diffusion regions used for short wires called "runners"

MOS transistor → 4 terminal device

C_G → intrinsic component (to body, Ⓢ, & Ⓓ (or Ⓢ alone dep. on operating regime).

→ overlap with Ⓢ & Ⓓ → $C_{diff.para}$ to body. ←



Scanned by CamScanner