SNS COLLEGE OF TECHNOLOGY

Coimbatore-35

An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE CODE & NAME: 16EC303 VLSI DESIGN

III YEAR/V SEMESTER

UNIT 1- MOS TRANSISTOR PRINCIPLE

TOPIC 3

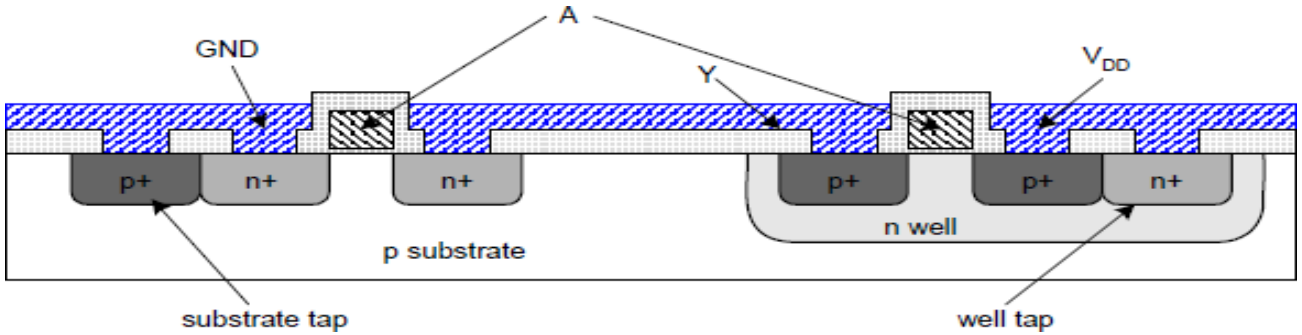
CMOS FABRICATION N-WELL PROCESS

OUTLINE

- CMOS Inverter in n-well process 1-8 steps
- Activity
- CMOS Inverter in n-well process 9-17 steps
- Inverter Cross section
- Mask levels
- Assessment
- Summary

N-WELL VS P-WELL

n-well: The pMOS transistors are placed in the n-well and the nMOS transistors are created on the substrate

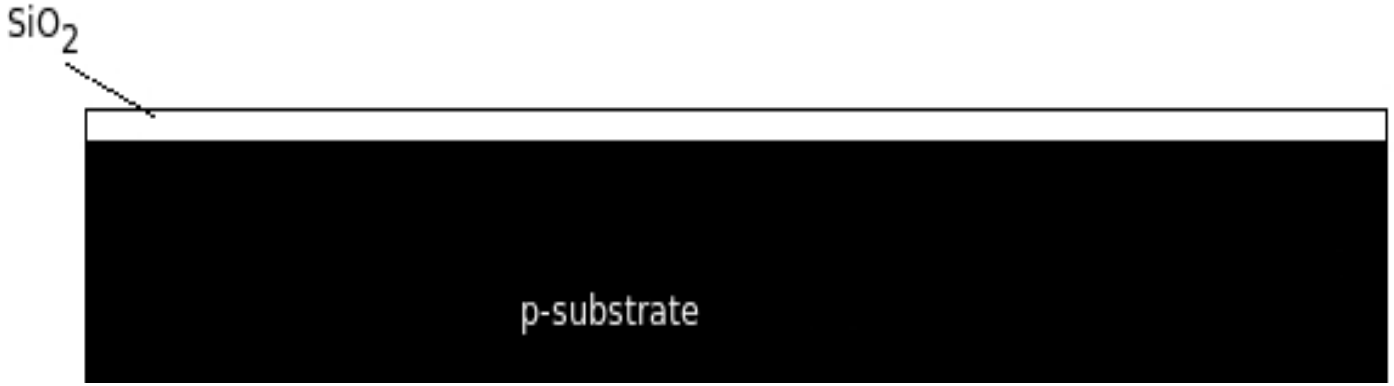


P-well: The nMOS transistors are placed in the p-well and the pMOS transistors are created on the substrate

1.WAFER

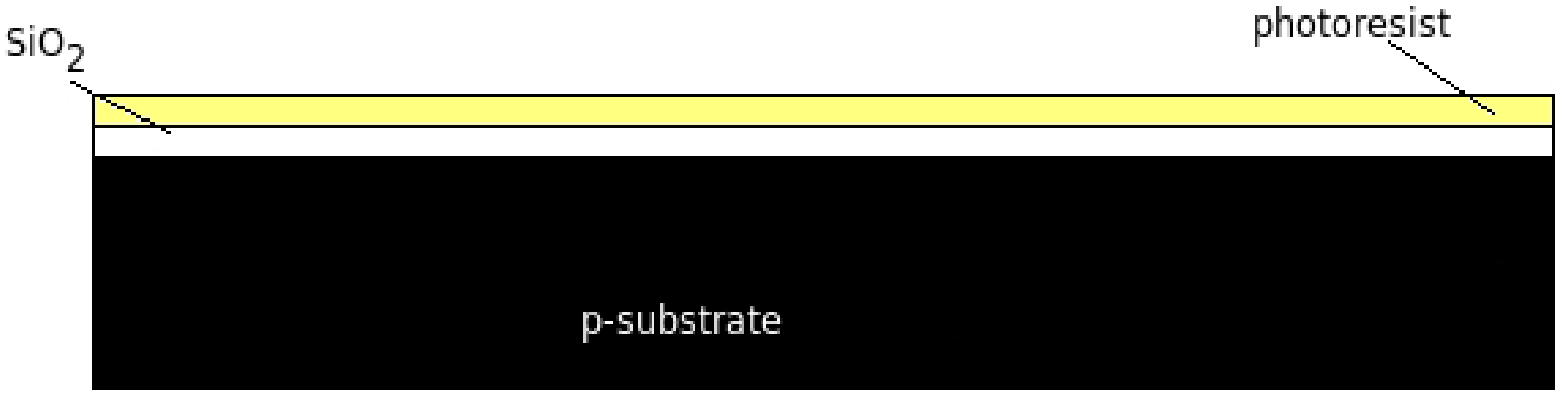
- A bare Si wafer is chosen
- The type will be n or p depending upon the technology

2.OXIDATION OF WAFER



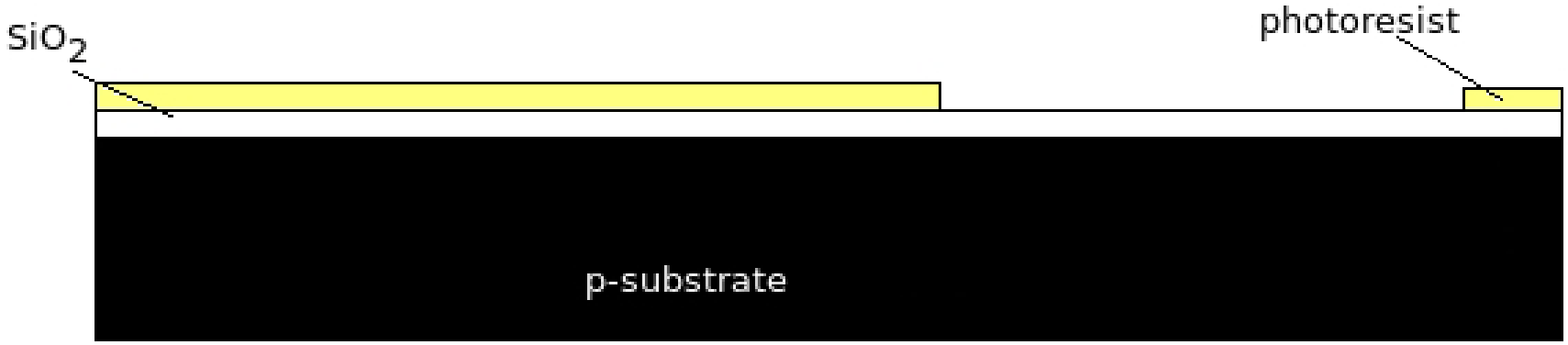
- The wafer is oxidised at a high temperature
- This must be patterned to define the n-well

3.PHOTORESIST DEPOSITION



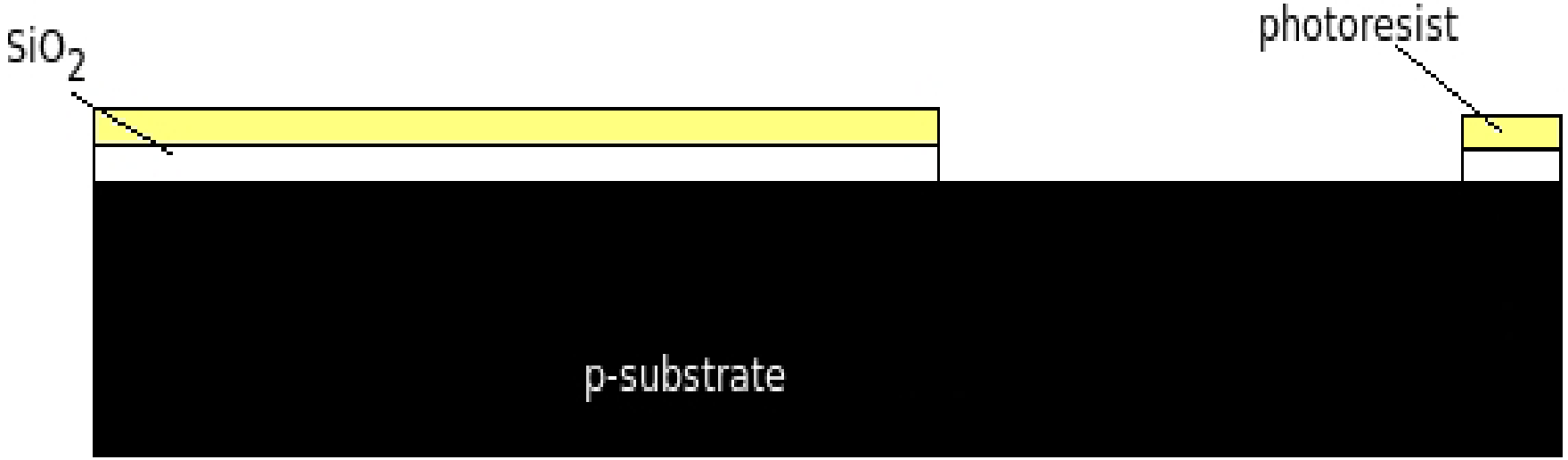
- The photoresist is deposited throughout the wafer
- The PR has to be patterned to allow formation of the well

4.N-WELL MASK



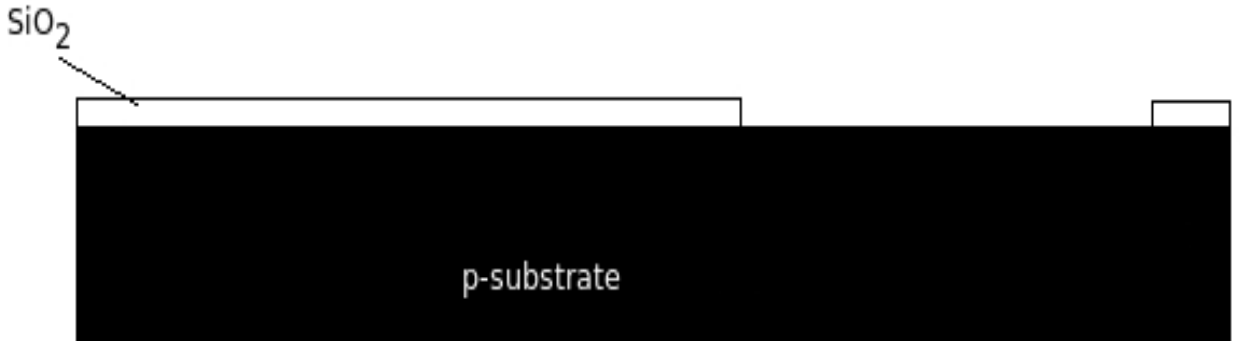
- The PhotoResist is exposed through the n-well mask
- The softened PhotoResist is is removed to expose the oxide

5.OXIDE ETCH



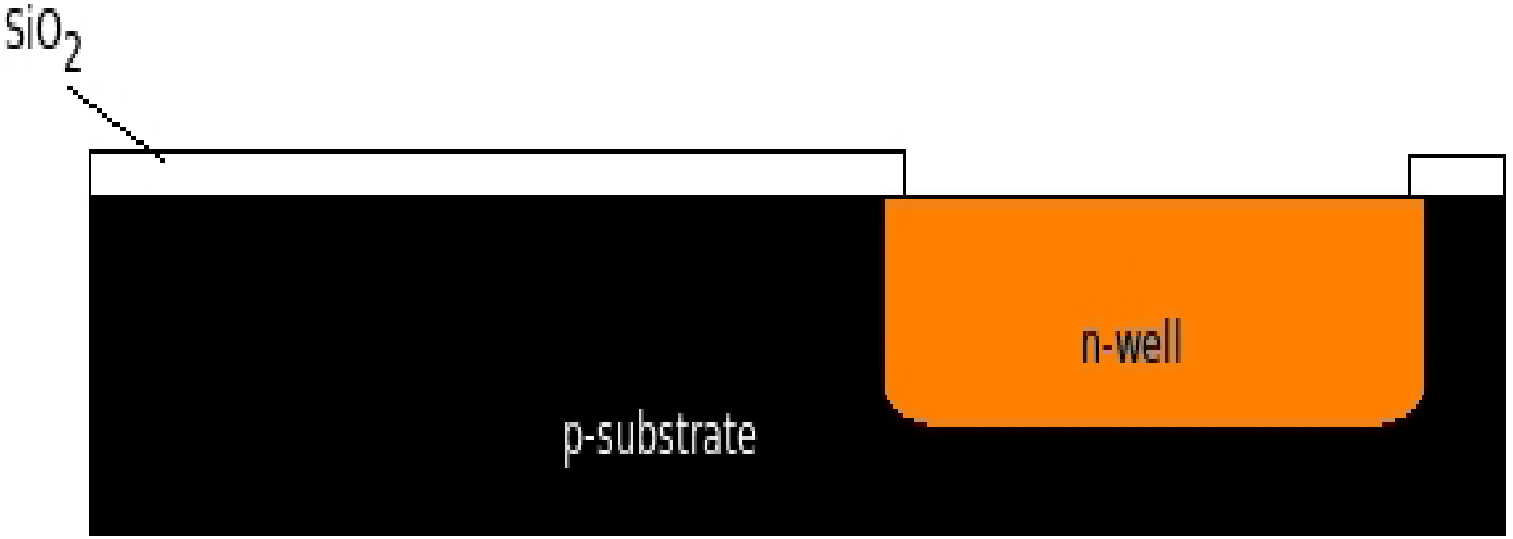
- The oxide is etched with HF acid where unprotected by Photo Resist
- The wafer is now exposed to the n-well area

6.PHOTORESIST REMOVAL



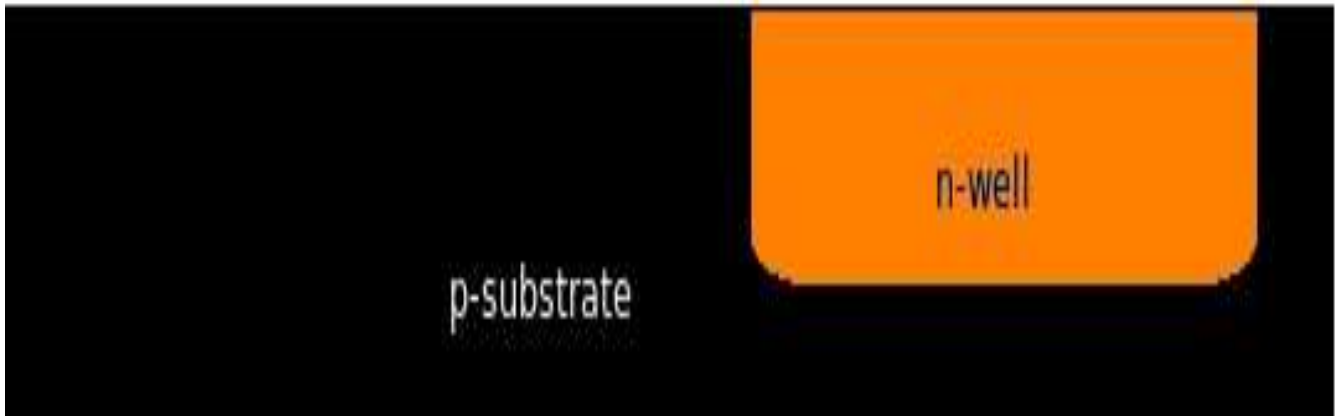
- The remaining PR is removed via piranha etch
- The well is ready to be formed

7.N-WELL FORMATION



- The diffusion process can make the the n-well
- Ion implantation can also form the same

8.OXIDE REMOVAL



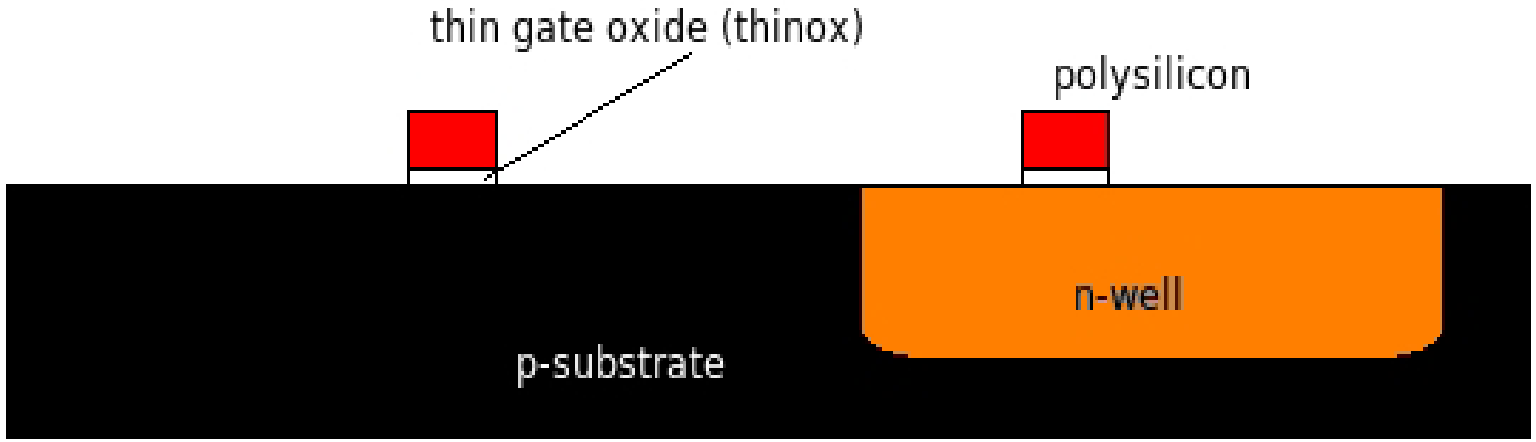
- The remaining oxide is stripped with HF acid
- This leaves the exposed wafer with the n-well formed

ACTIVITY

Connections

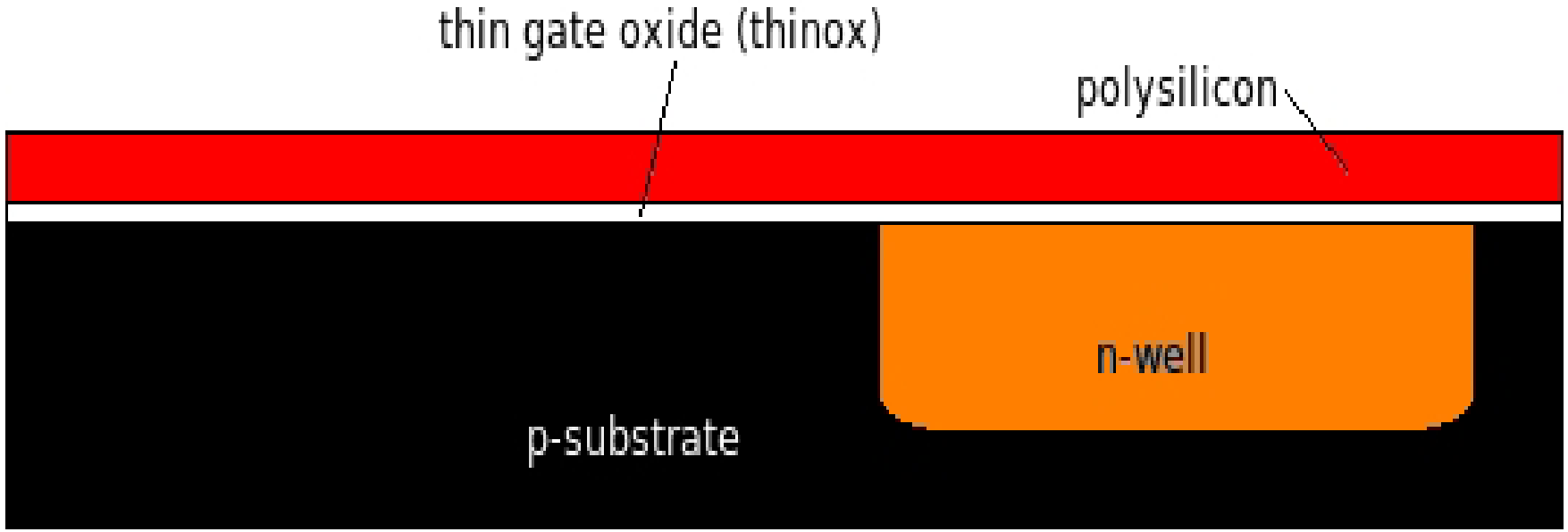
Start the word from Electronics..Next starting letter is S

9.GATE FORMATION



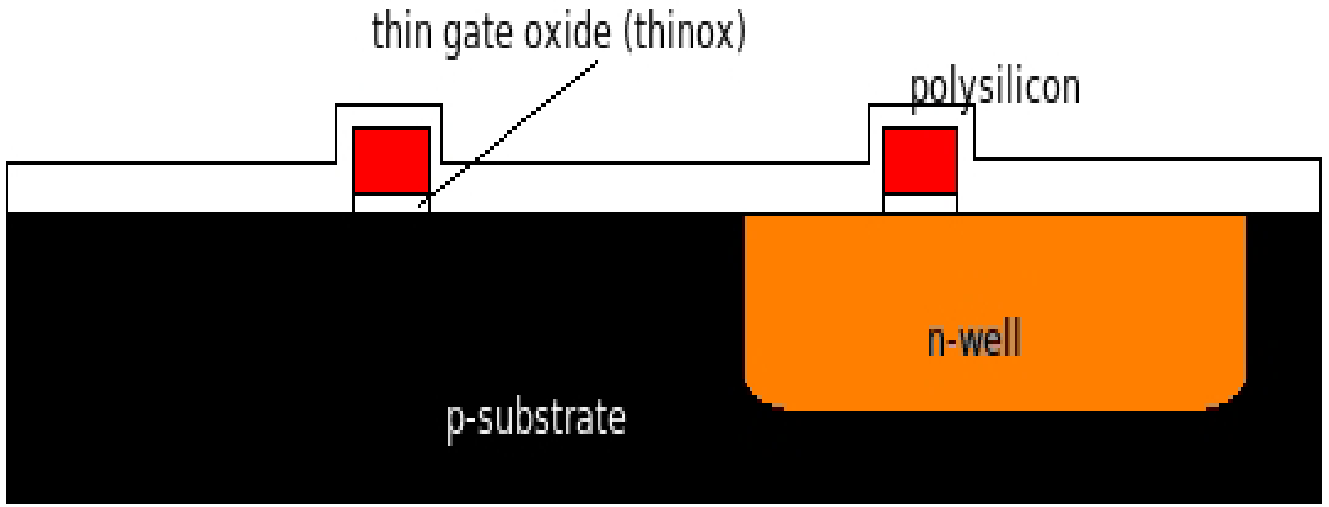
- The gates are made up of polysilicon over thinox
- CVD is used to grow the poly (heavily doped) layer

10.POLY PATTERNING



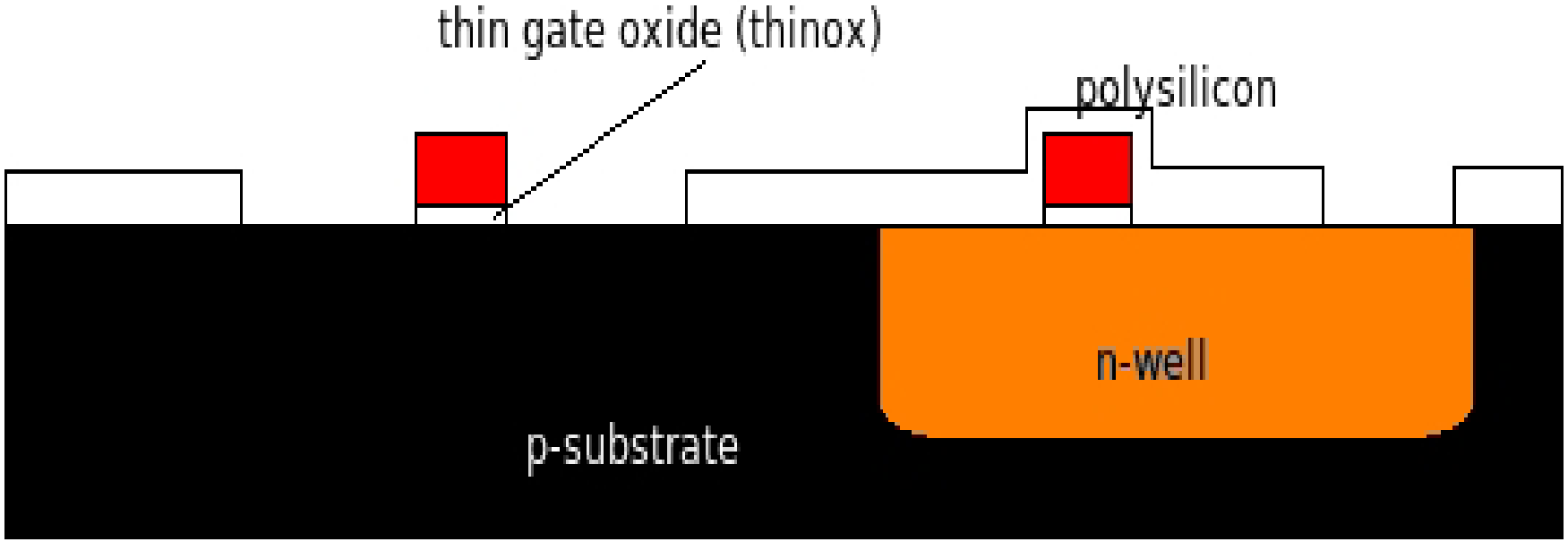
- The wafer is now patterned with PhotoResist and the poly mask
- Finally this leaves the device gates

11.DIFFUSION PATTERN



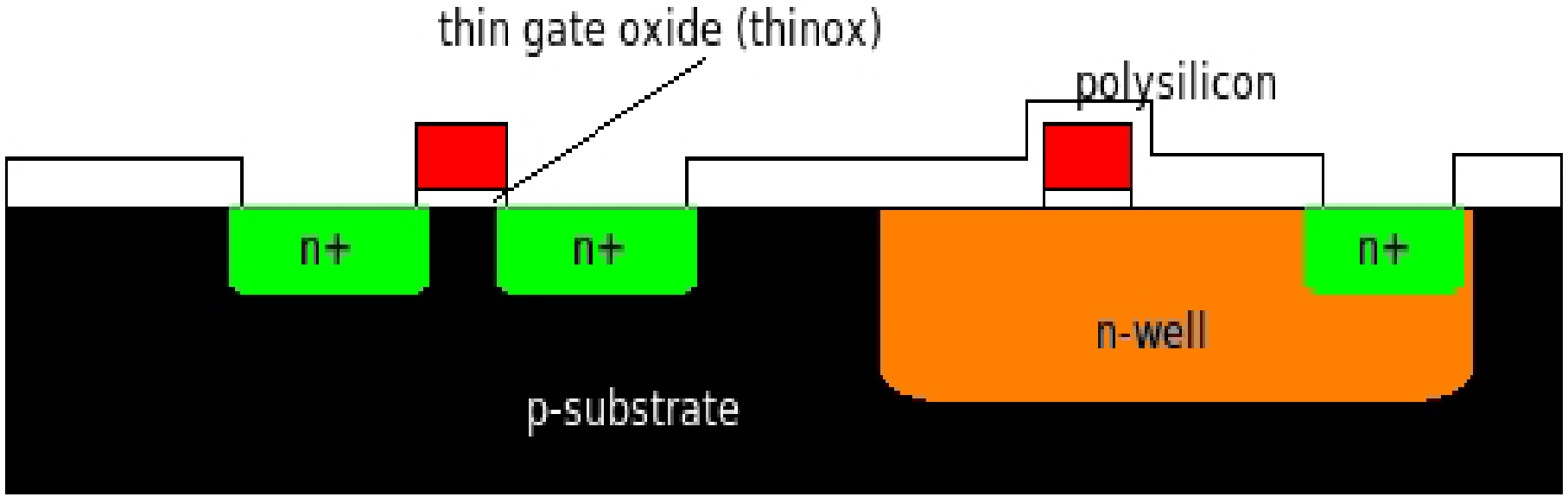
- Again, a protective oxide is grown and PhotoResist deposited
- PhotoResist is patterned according to the diffusion mask

12.WAFER EXPOSURE FOR DIFFUSION



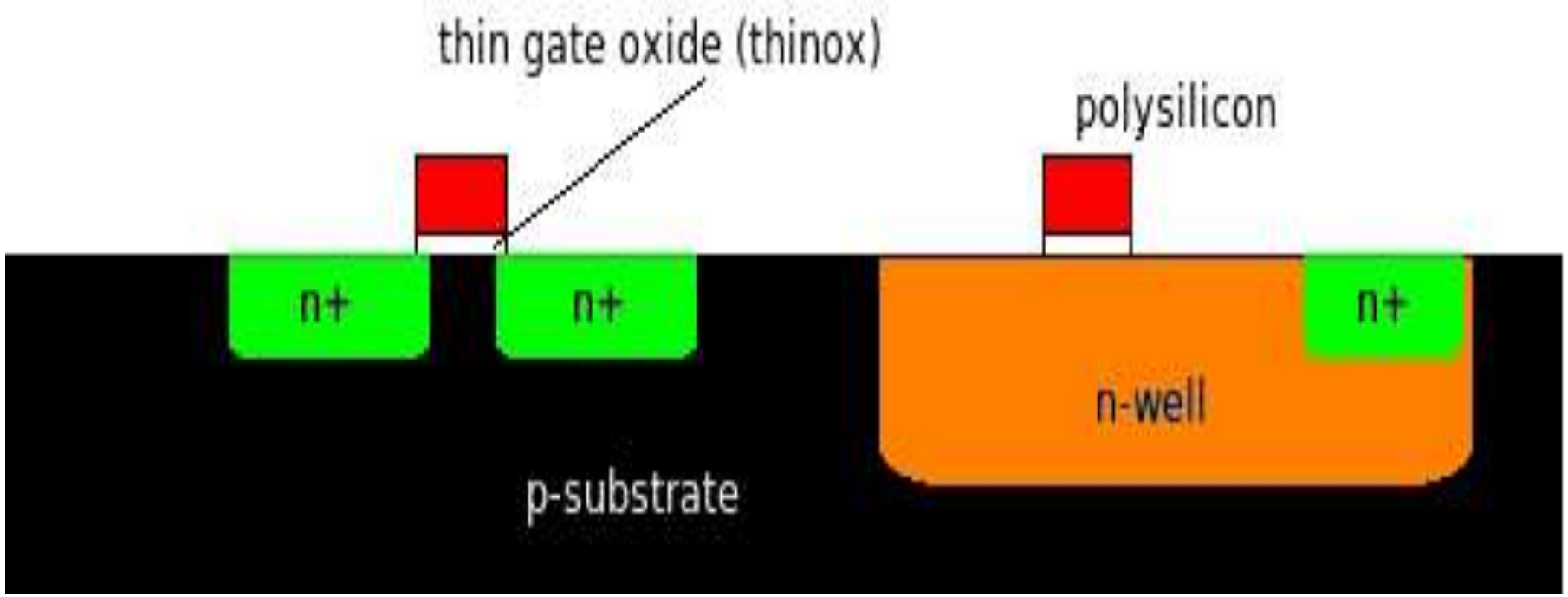
- The protective oxide is etched away
- The wafer is exposed for S/D formation

13.N-DIFFUSION REGIONS



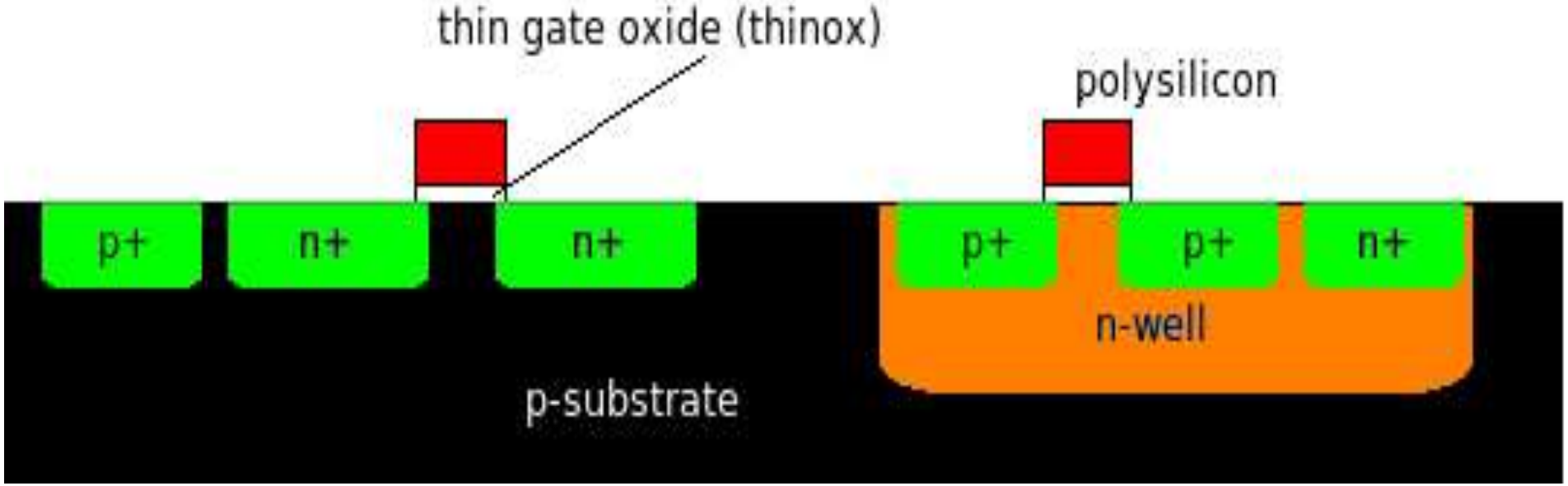
- The n+ diffusion regions are formed
- Polysilicon blocks the channel area

14.SELF-ALIGNED PROCESS



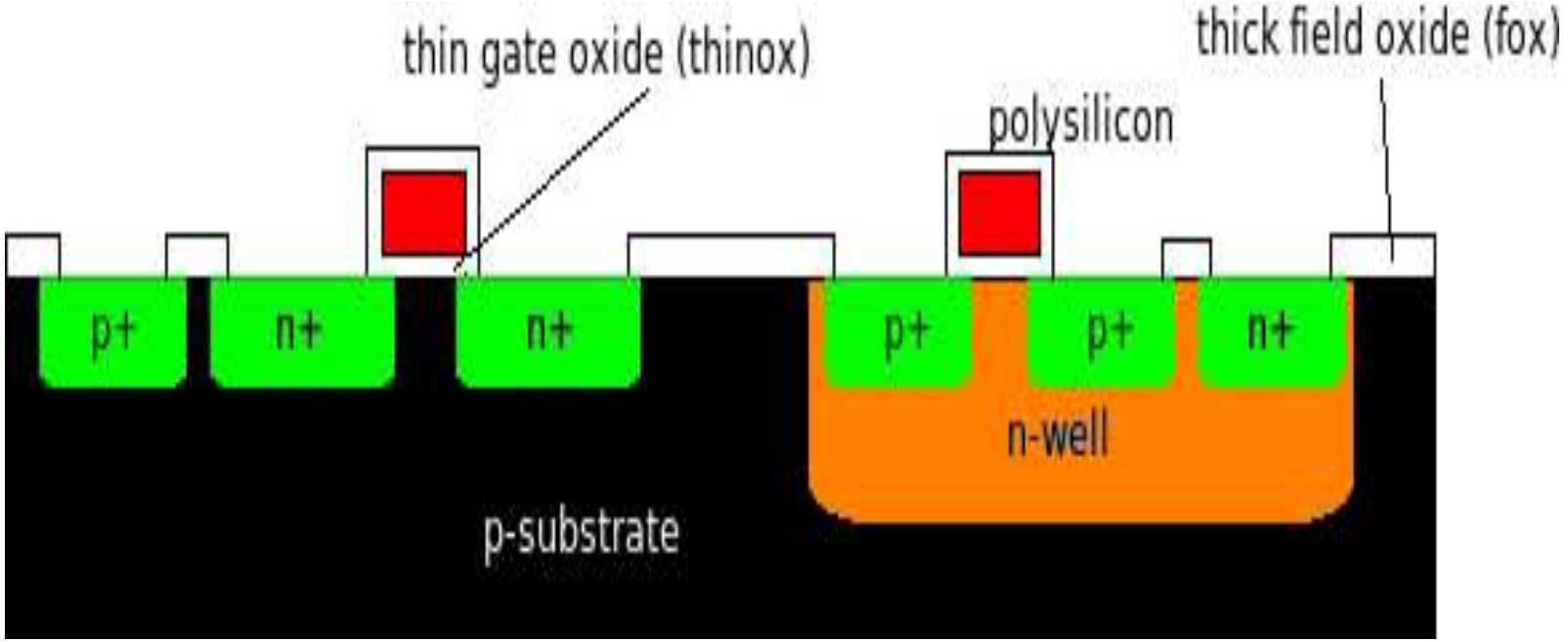
- This is a self-aligned process
- S/D are automatically formed adjacent to the gate

15.P-DIFFUSION



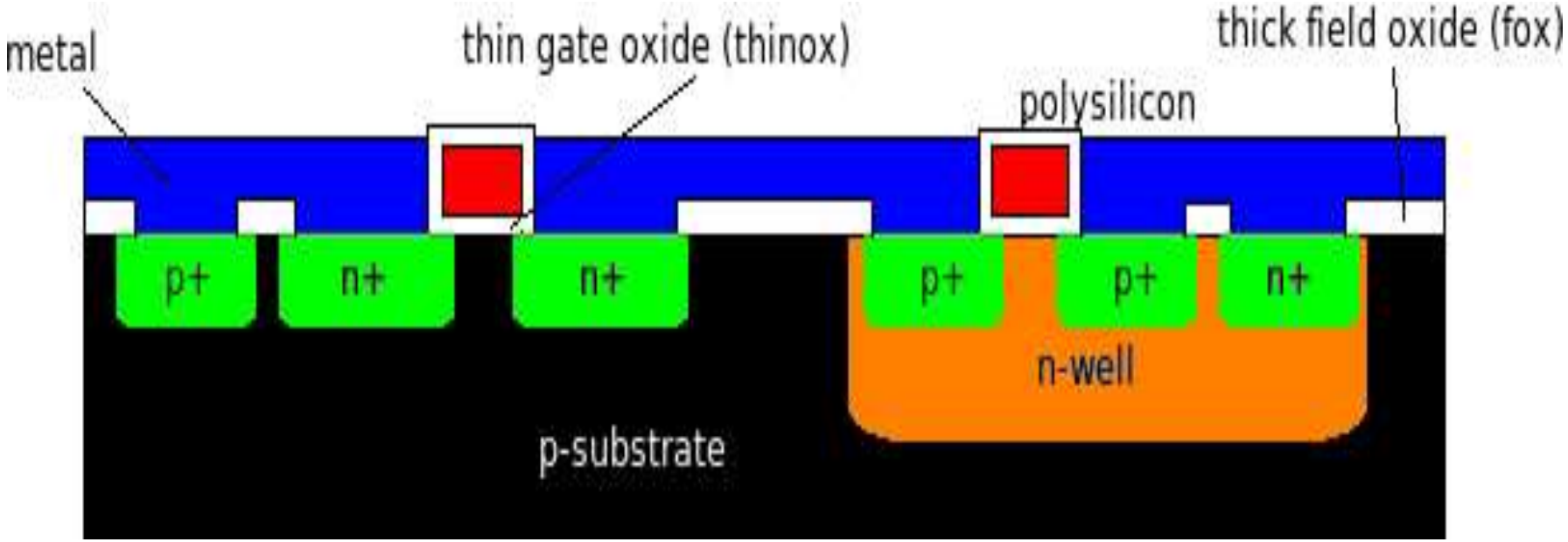
- The p-diffusion mask is used next
- This completes creation of all active regions

16.Field Oxide



- The field oxide is grown to insulate wafer and metal
- It is patterned with the contact mask

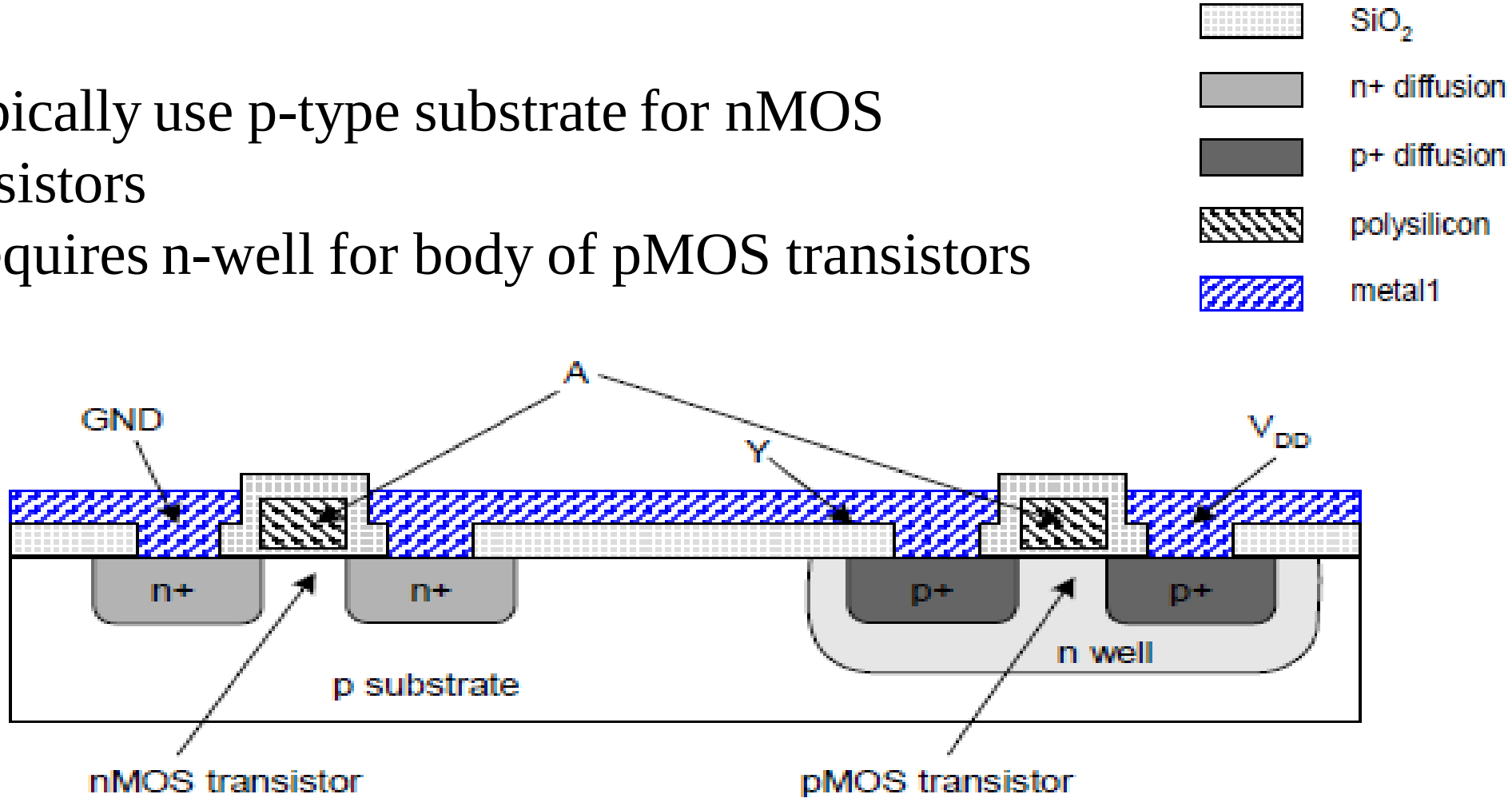
17.METAL FORMATION



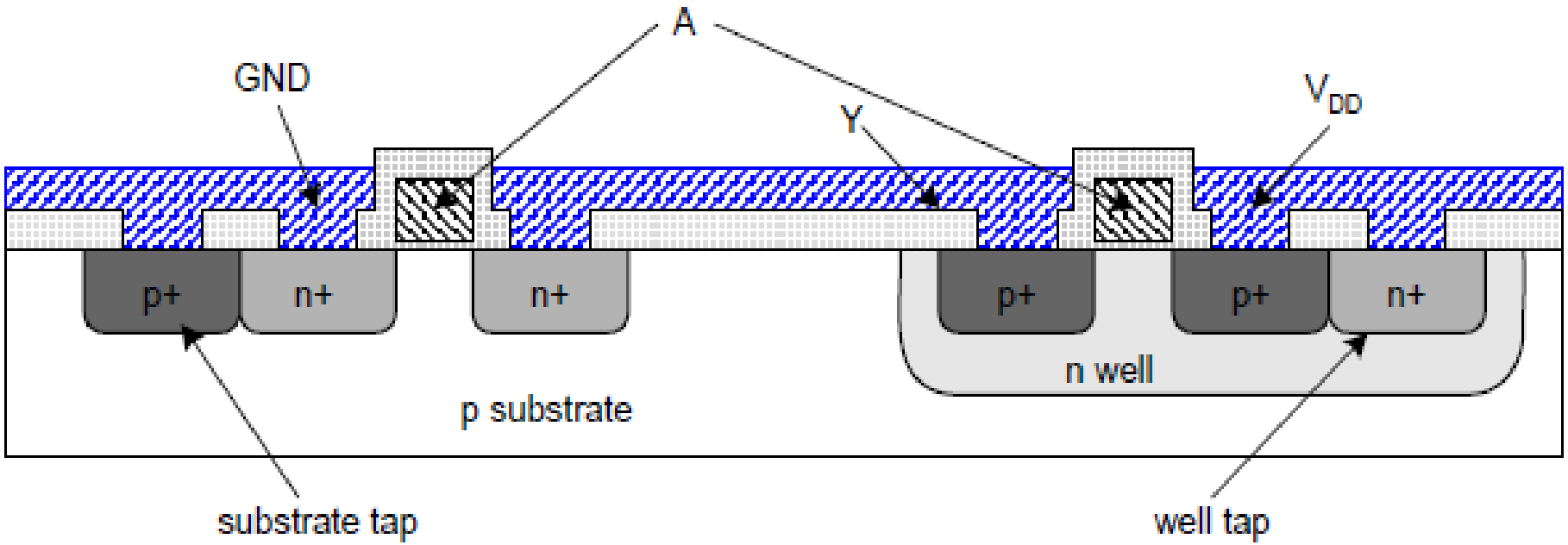
- Al is sputtered over the entire area filling contact cuts too
- Metal is patterned with the metal mask

INVERTER CROSS-SECTION

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors

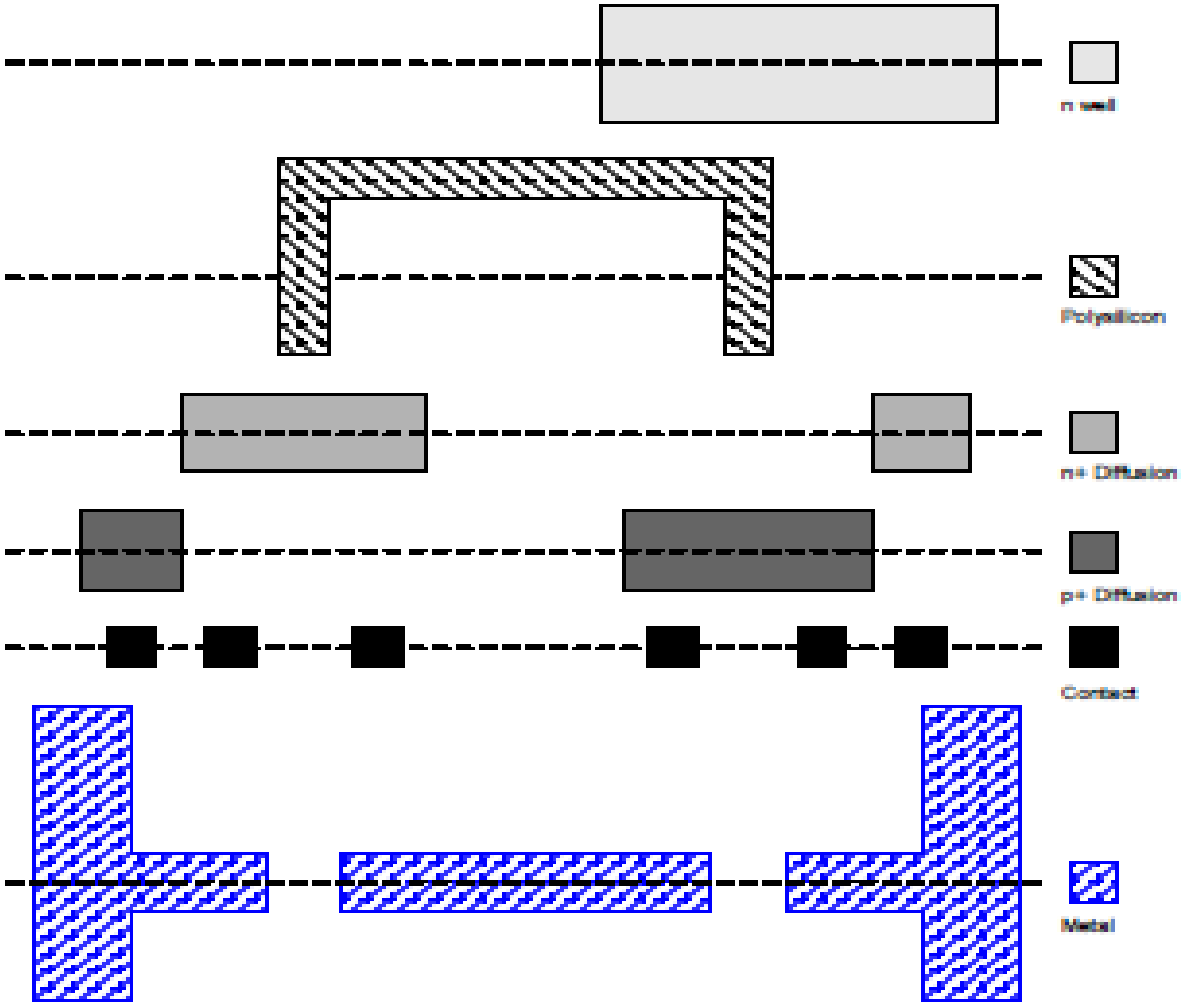


WELL AND SUBSTRATE TAPS



- Substrate must be tied to GND, n-well to VDD
- Use heavily doped well and substrate contacts / taps

SIX MASKS



- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal

ASSESSMENT

1.Six masks-Fill the missed steps

n-well

- - - - - - - -

–---diffusion

–----diffusion

– Contact

– Metal

2. Tell me the n-well EVEN steps

3. Tell me the n-well ODD steps


THANK
YOU!