



SNS COLLEGE OF ENGINEERING
(Autonomous)
DEPARTMENT OF CSE - IoT



COURSE NAME:19EC306 / DIGITAL CIRCUITS
II YEAR/III SEMESTER

UNIT:1- MINIMIZATION TECHNIQUES AND LOGIC GATES

TOPIC:BOOLEAN POSTULATES AND LAWS



Outline

- Interpretation of Boolean Algebra using Logic Operations
- Boolean Algebra and Gates
- Theorems and Proofs



Section 1: Interpretation of Boolean Algebra using Logic Operations



Logic Symbols, 0, 1; and AND, OR Gates.

$a = 1 \Rightarrow$ a is true ,

$a = 0 \Rightarrow$ a is false.

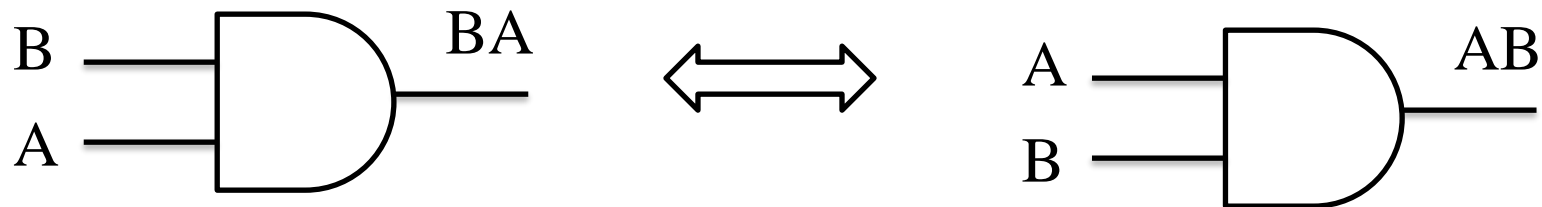
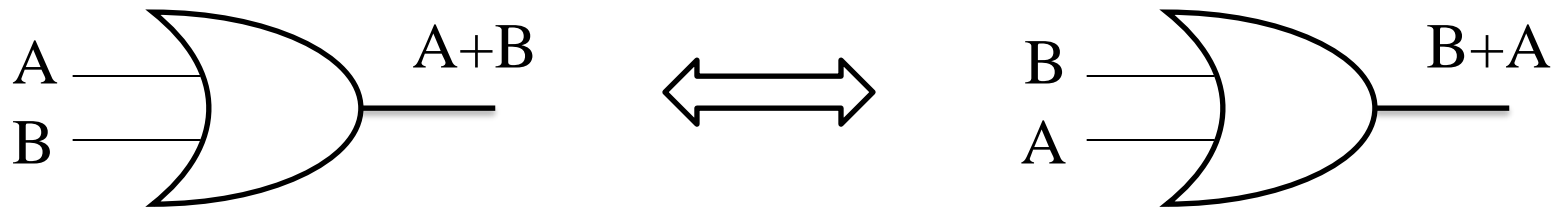
<i>id</i>	<i>a</i>	<i>b</i>	<i>a OR b</i>
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

<i>Id</i>	<i>a</i>	<i>b</i>	<i>a AND b</i>
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1



Section 2: Boolean Algebra and Gates

P1: Commutative Laws





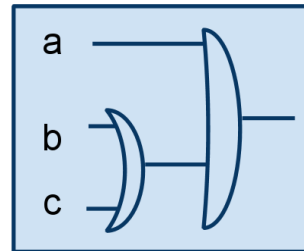
P2: Distributive Laws

- $a \cdot (b+c) = (a \cdot b) + (a \cdot c)$
- $a + (b \cdot c) = (a+b) \cdot (a+c)$

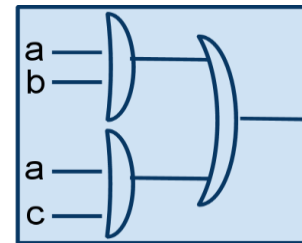
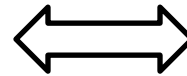
ID	a	b	c	b+c	$a \cdot (b+c)$		a · b	a · c	$(a \cdot b) + (a \cdot c)$
0	0	0	0	0	0		0	0	0
1	0	0	1	1	0		0	0	0
2	0	1	0	1	0		0	0	0
3	0	1	1	1	0		0	0	0
4	1	0	0	0	0		0	0	0
5	1	0	1	1	1		0	1	1
6	1	1	0	1	1		1	0	1
7	1	1	1	1	1		1	1	1



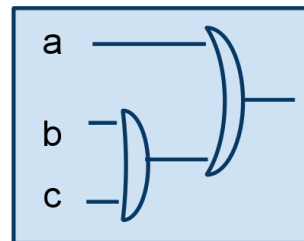
P2: Distributive Laws, cont.



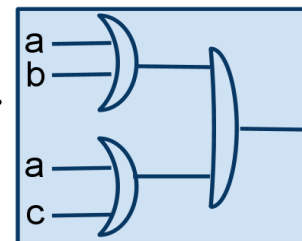
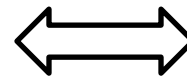
$$a \cdot (b + c)$$



$$(a \cdot b) + (a \cdot c)$$



$$a + (b \cdot c)$$



$$(a + b) \cdot (a + c)$$



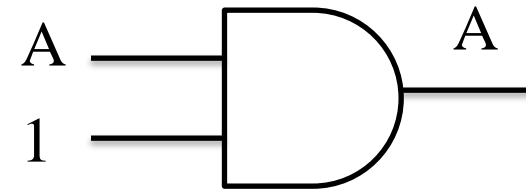
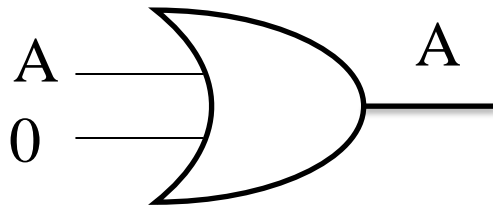
P3 Identity

$$a+0 = a,$$

$$a \cdot 1 = a,$$

0 input to OR is passive

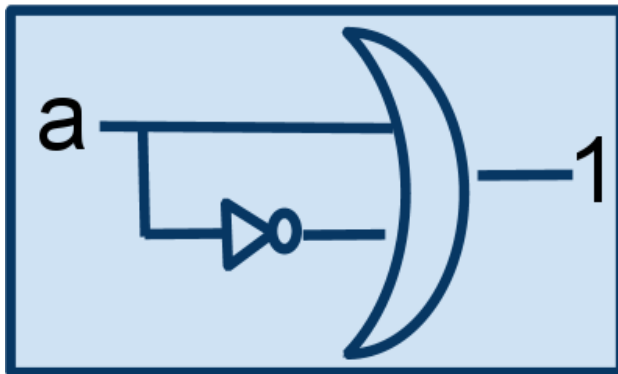
1 input to AND is passive



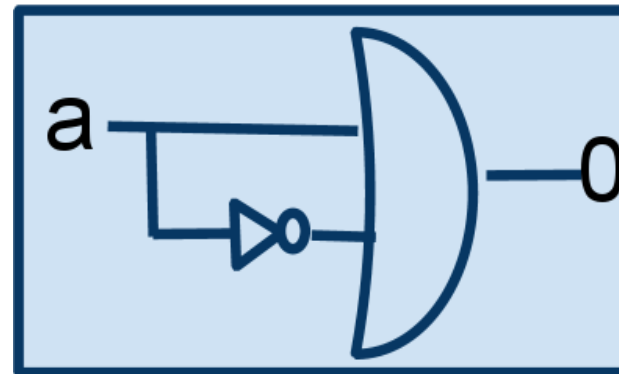


P4 Complement

$$a + a' = 1$$



$$a \cdot a' = 0$$





Section 3, Theorems and Proofs



Theorem 1: Principle of Duality

- Every algebraic identity that can be proven by Boolean algebra laws, remains valid if we swap all '+' and '.', 0 and 1.

Proof:

- Visible by inspection – all laws remain valid if we interchange all
 '+' and '.', 0 and 1



Theorem 2

Uniqueness of Complement: For every a in B , its complement a' is unique.

Proof: We prove by contradiction.

Suppose that a' is not unique, i.e. a_1' , a_2' in B & $a_1' \neq a_2'$.

$$\begin{aligned} \text{We have } a_1' &= a_1' * 1 \text{ (Postulate 3)} \\ &= a_1' * (a + a_2') \text{ (Postulate 4)} \\ &= (a_1' * a) + (a_1' * a_2') \text{ (Postulate 2)} \\ &= 0 + (a_1' * a_2') \text{ (Postulate 4)} \\ &= a_1' * a_2' \text{ (Postulate 3)}. \end{aligned}$$

Likewise, we can also prove the same with a_2' , i.e.

$$a_2' = a_1' * a_2'.$$

Consequently, we have $a_1' = a_2'$, which contradicts our initial assumption that $a_1' \neq a_2'$.



Theorem 3

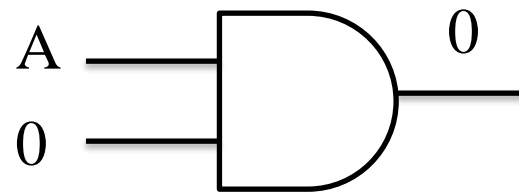
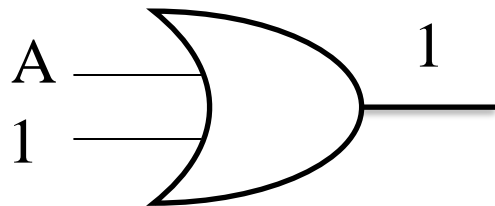
Boundedness: For all elements a in B , $a+1=1$;
 $a*0=0$.

$$\begin{aligned} \text{Proof: } a+1 &= 1 * (a+1) && \text{(Postulate 3)} \\ &= (a + a') * (a+1) && \text{(Postulate 4)} \\ &= a + a' * 1 && \text{(Postulate 2)} \\ &= a + a' && \text{(Postulate 3)} \\ &= 1 && \text{(Postulate 4)} \end{aligned}$$

Comments:

'1' dominates as input in OR gates.

'0' dominates as input in AND gates.





Theorem 4

Statement:

- The complement of element 1 is 0 and vice versa, i.e.

$$0' = 1, 1' = 0.$$

Proof:

$$0 + 1 = 1 \text{ and } 0 * 1 = 0 \text{ (Postulate 3)}$$

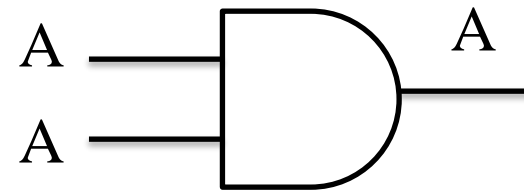
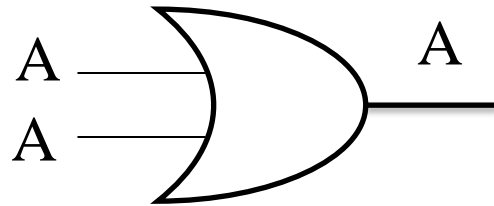
Thus $0' = 1, 1' = 0$ (Postulate 4 and Theorem 2)



Theorem 5: Idempotent Laws

Statement: For every a in B ,

$$a + a = a \quad \text{and} \quad a * a = a.$$



Proof:

$$\begin{aligned} a + a &= (a + a) * 1 && \text{(Postulate 3)} \\ &= (a + a) * (a + a') && \text{(Postulate 4)} \\ &= a + (a * a') && \text{(Postulate 2)} \\ &= a + 0 && \text{(Postulate 4)} \\ &= a && \text{(Postulate 3)} \end{aligned}$$



Thank
you

11/09/23

Minimization techniques and logic gates/19EC306 –Digital
Circuits/Dr. J. Grace Jency/CSE - IoT/SNSCE
Minimization techniques and logic
gates/19EC306 –Digital
Circuits/S.Jayashree/CSD/SNSCE