SNS COLLEGE OF ENGINEERING

(Autonomous)

DEPARTMENT OF CSE - IoT

COURSE NAME:19EC306 / DIGITAL CIRCUITS

II YEAR/III SEMESTER

UNIT:1- MINIMIZATION TECHNIQUES AND LOGIC GATES

TOPIC:SUM OF PRODUCTS & PRODUCTS OF SUM

Karnaugh map - Outline

- Feel a little difficult using Boolean algebra laws, rules, and theorems to simplify logic?
- A K-map provides a systematic method for simplifying Boolean expressions and, if properly used, will produce the simplest SOP or POS expression possible, known as the minimum expression.

K – Map – SOP Reduction

- After an SOP expression has been mapped, we can do the process of *minimization:*
  - Grouping the 1s
  - Determining the minimum SOP expression from the map

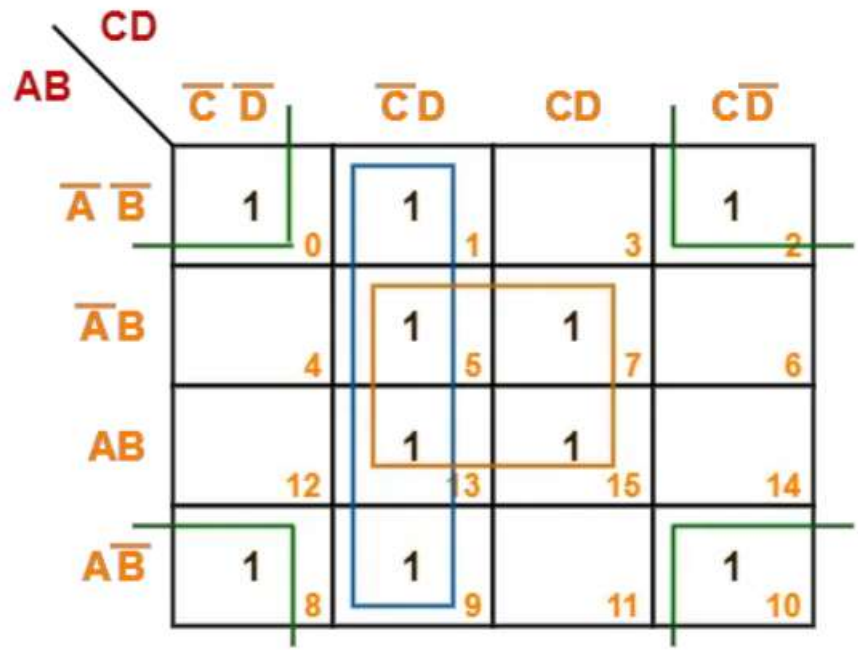
- You can group 1s on the K-map according to the following rules by enclosing those adjacent cells containing 1s.
- **The goal** is to maximize the size of the groups and to minimize the number of groups.

K – Map – SOP Reduction

Minimize the following boolean function-

$$F(A, B, C, D) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$$

Then, we have-



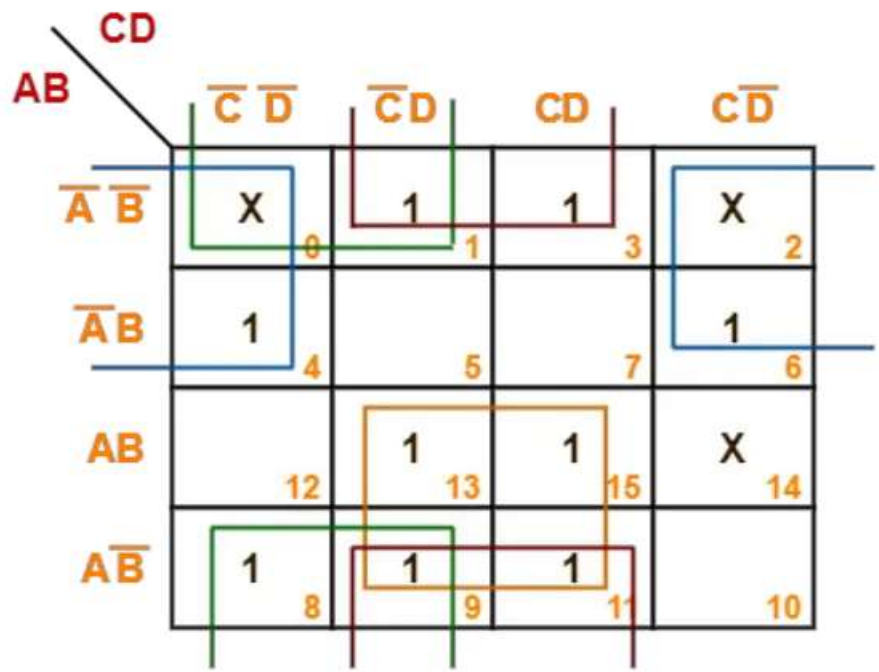
Thus, minimized boolean expression is-

F(A, B, C, D) = BD + C'D + B'D'

K- Map Examples

Minimize the following boolean function-

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$$

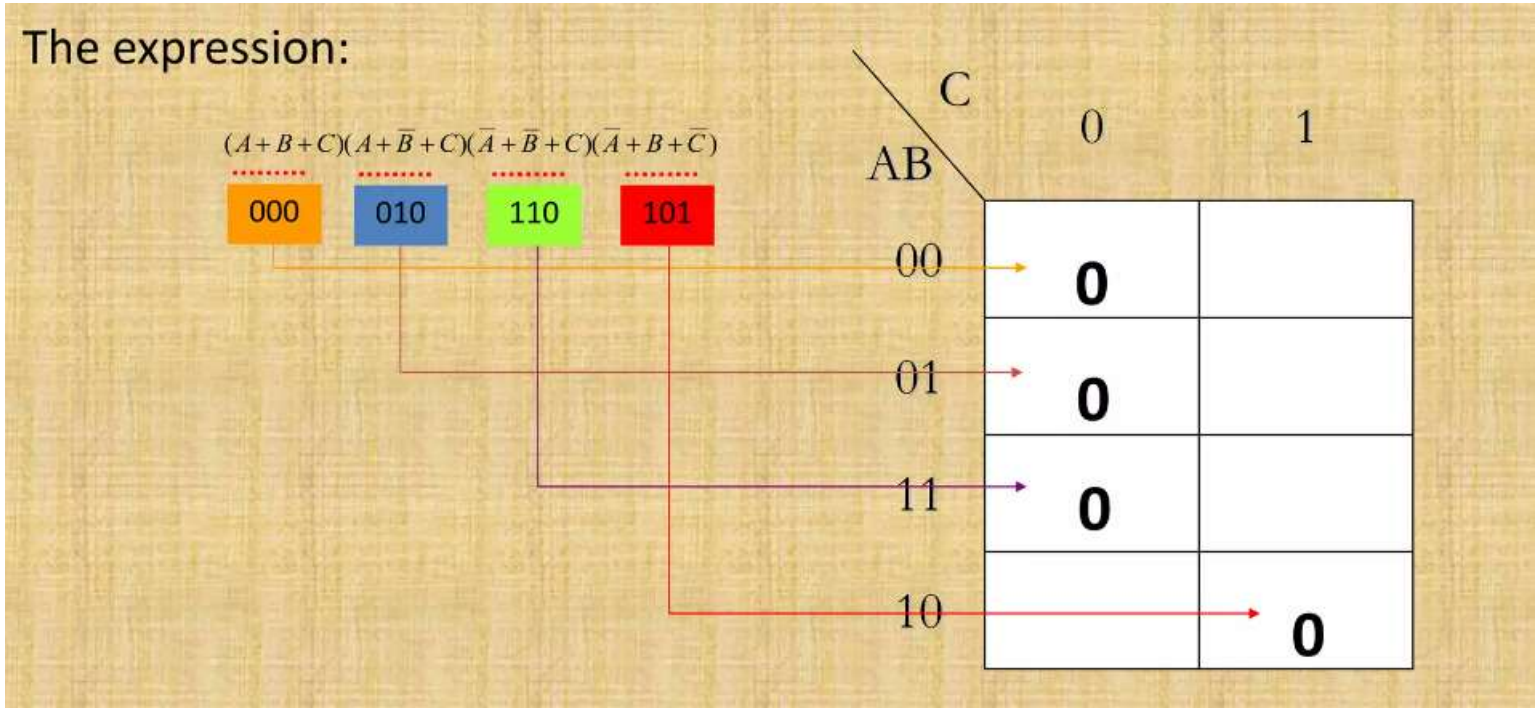


Thus, minimized boolean expression is-

F(A, B, C, D) = AD + B'D + B'C' + A'D'

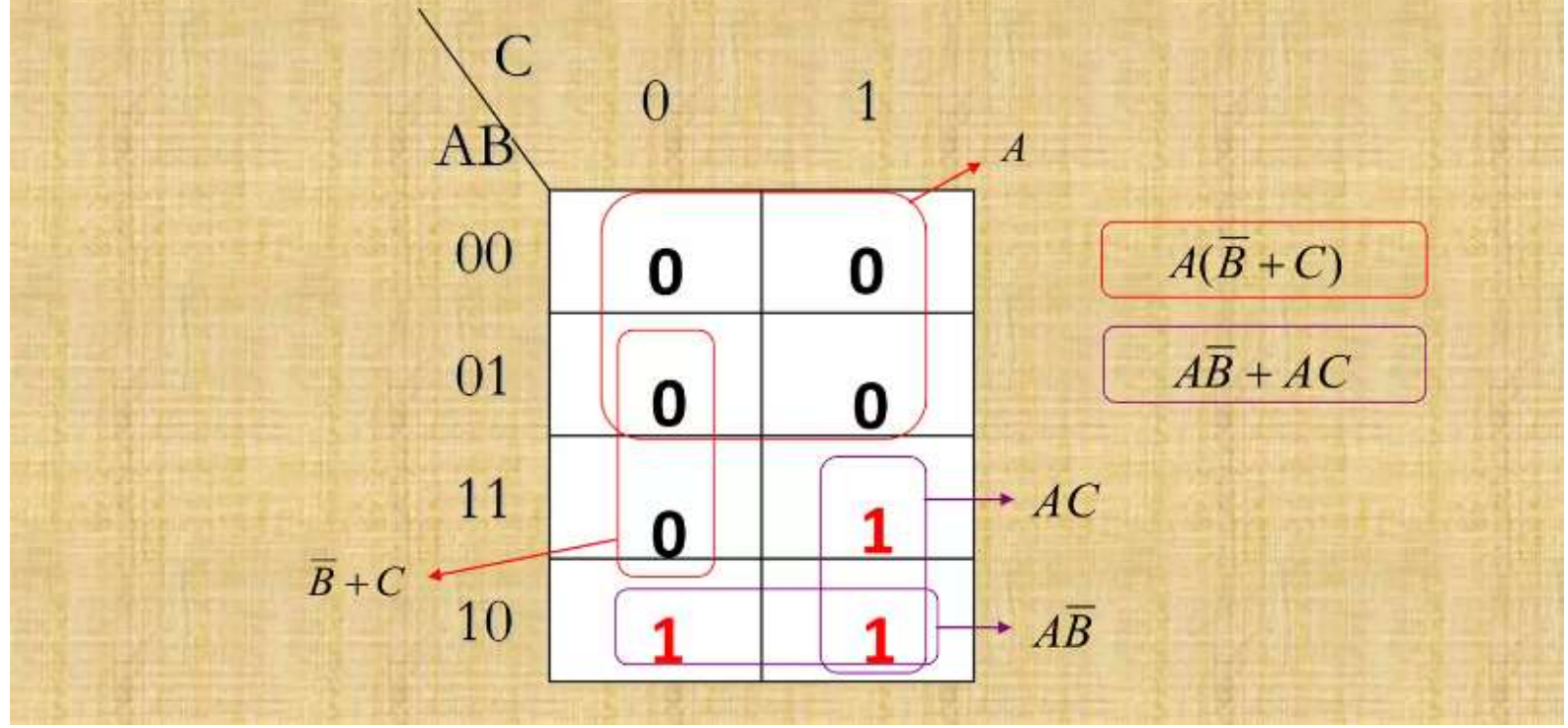
K – Map – POS Reduction

- The approaches are much the same (as SOP) except that with POS expression, 0s representing the standard sum terms are placed on the K-map instead of 1s.



Contd….

$(A+B+C)(A+B+\overline{C})(A+\overline{B}+C)(A+\overline{B}+\overline{C})(\overline{A}+\overline{B}+C)$



Design of combinational digital circuit

- From the problem statement derive the truth table
- From the truth table derive the unsimplified logic expression
- Simplify the logic expression
- From the simplified expression draw the logic circuit


Thank you