Roll No. | | | | | | | | | | | | |

Total No. of Questions: 09 **Total No. of Pages: 02**

B. Tech. ECE/(EE/EEE)/EIE (Sem. 4)
DIGITAL ELECTRONICS
Subject Code: EC-204
Paper ID: A0307

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **Section A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **Section B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **Section C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1. Explain briefly:

a) Convert to BNS to grey code (11110001101).

b) $(213)_8$ - $(145)_8$ $=(------)_8$ and $(2FC)_{16}$ + (I CD)$_{16}$=$(------)_{16}$

c) What is race around condition and how it is improved.

d) Subtract using 2's and l's complement (34-14).

e) Solve $(185)_8$=$(------)_{10}$ and $(ADF)_{16}$ =$(------)_2$

f) What is the difference between combinational and sequential circuits.

g) What are the advantages of TTL over DTL

h) What are the applications of ring counter.

i) Explain terms fan-in, fan-out and Resolution AD Converter.

j) What are the applications of Multiplexer?

SECTION B

2. Solve using K-map and implement using NAND gates only.

F(v,w,x,y)= Πm (0,1,2, 7,9,l l,14,15)+d(4,5)

3. Design full adder using 4:1 Multiplexer and 8:1 MUX.

4. Design four bit binary number system to grey code converter.

5. Explain-working of CMOS NAND gate in detail.

6. Explain the working of voltage to time conversion circuit.

SECTION C

7. Solve using Q-M method and verify the result with K-map. Also implement using NOR gates only.

F(v,w,x,y,z)= Σm (0,1,2,4,5 ,14,15,19,23,25,27,29,31)+d(7,8,9,l l)

8. (a) Explain the working single slope AID converter.

(b) Design MOD-5 counter using JK Flip-flops.

9. Design MOD-6 up-down counter using D flip-flops.