Roll No. | | | | | | | | | | | | | **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(ECE)/(EE/EEE)/(EIE) (Sem.–4)

DIGITAL ELECTRONICS

Subject Code : EC-204

Paper ID : [A0307]

Time : 3 Hrs. **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. Write briefly :

a) What is a weighted code, give two examples?

b) Perform the BCD addition of 67and 58.

c) Compare a canonical and slandered form.

d) What is a parity checker?

e) Write excitation table of a J-K and D flip-flop.

f) Compare a synchronous and asynchronous counter.

g) Define resolution and accuracy of D/A converter.

h) Compare a PLA and PAL.

i) Define tri-state logic.

j) What is wired AND gate?

SECTION-B

2. In a new number system X and Y are successive digits such that $(XY)_r = (25)_{10}$ and $(XY)_r = (31)_{10}$ find X, Y, r.

3. Reduce to its minimum sum of products form using theorems only X = A'B'C'D' + A'B'CD' + AB'C'D' + A'CD + AB'CD'

4. Implement the following function using 4×1 multiplexer $y = \Sigma m(0, 2, 6, 8, 9, 11,13,15)$

5. What is a dual slope A/D converter? Draw its circuit and explain its working.

6. A ripple counter uses flip-flops having t_{pd} = 12 ns. What can be the largest mode counter constructed from flip-flops and operated at 10 MHz?

SECTION-C

7. Explain the reading and writing process in a typical Bipolar RAM cell.

8. Give the classification of TTL. Explain working of a totem pole TTL.

9. Design a BCD synchronous up/down counter using J-K flip-flop.