Roll No. ☐☐☐☐☐☐☐☐☐☐☐   **Total No. of Pages : 02**

Total No. of Questions : 09

B.Tech.(ECE)/(EE/EEE)/(EIE)   (Sem.–4)

DIGITAL ELECTRONICS

Subject Code : EC-204

Paper ID : [A0307]

Time : 3 Hrs.   **Max. Marks : 60**

INSTRUCTIONS TO CANDIDATES :
1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION-A

1. **Write briefly :**

   1. Subtract (23-17) using 2's and 1's complement.

   2. Explain term Resolution and accuracy of D/A converter.

   3. What is difference between synchronous and ripple counter.

   4. What is race around condition and how it is improved?

   5. Give the characteristics table of RS and D Flip-flop.

   6. Explain difference between combinational and sequential circuits.

   7. What are the advantages of CMOS over DTL?

   8. Add two BCD numbers 435+375.

   9. Explain difference between static and dynamic memory.

   10. Explain the function of PRESET and CLEAR in Flip-flop.

SECTION-B

2. Design a BCD to Grey code converter circuit.

3. Explain the working of simultaneous and counter type A/D converter in detail.

4. Explain the totem pole TTL NAND logic families in detail.

5. Explain 3 bit Asynchronous counter using wave form and design MOD-14 Ripple Counter.

6. Solve using K map and implement with the help of NAND gates only

   $F_{(v, w, x, y)} = \prod m(0,1,2,3,8,10,11) + d(13,14,15)$

SECTION-C

7. Solve using K-map and Q-M methods and implement using NAND gates only.

   $F_{(v, w, x, y, z)} = \sum m(0,1,2,3,9,10,12,16,18,19,29,31) + d(13,14,26)$.

8. Design a MOD-6 up-down counter using JK Flip-flop by avoiding lockout conditions.

9. Write a short note on **any two** :

   a. Ring counter and Johnson counter.

   b. Voltage of frequency conversion

   c. PLA