Total No. of Questions: 09

B.Tech. (ECE)/(EE/EEE)/(EIE) (2010 Batch Only) (Sem. – 4)

DIGITAL ELECTRONICS

M Code: 57011
Subject Code: EC-204
Paper ID: [A0307]

Time: 3 Hrs. **Max. Marks: 60**

INSTRUCTIONS TO CANDIDATES:

1. **SECTION-A is COMPULSORY consisting of TEN questions carrying TWO marks each.**
2. **SECTION-B contains FIVE questions carrying FIVE marks each and students have to attempt any FOUR questions.**
3. **SECTION-C contains THREE questions carrying TEN marks each and students have to attempt any TWO questions.**

SECTION A

1. a) Add hexadecimal numbers 2EC and 3A4.

   b) Represent decimal number 6027 in BCD and Excess-3 codes.

   c) Convert to POS form F = $xy + \bar{x}z$.

   d) Explain Demorgan's Laws.

   e) What is a full subtractor? Give its truth table.

   f) What is race around condition? What is its solution?

   g) A digital to analog converter has a maximum output of 15V. Determine the resolution and permissible error for 8-bits.

   h) Compare PLAs and PALs.

   i) What do you mean by terms "fan in" and "fan out"?

   j) Explain the noise margin, and advantages of CMOS.

SECTION B

2. Solve the function $F_{(ABCD)} = \sum m\ (0, 1, 2, 3, 5, 7, 8, 10, 14, 15)$ using Q-M method.
3. Design BCD to grey code combinational circuit.
4. How will you convert R-S flip flop into J-K flip flop? Also discuss characteristic table of J-K Flip flop.
5. What is the difference between ROM and RAM? Draw the basic structure of RAM cell. Compare static and dynamic RAM cells.
6. Explain the principles of operation of Counter type ADC and Single slope ADC.

SECTION C

7. Design a counter with the repeated binary sequence: 0, 1, 2, 3, 4, 5, 6 using J-K flip flop by avoiding lock out condition.
8. Design 2-bit magnitude comparator combinational circuit.
9. Write notes on following:

   a) ECL and DTL logic families

   b) Shift Registers