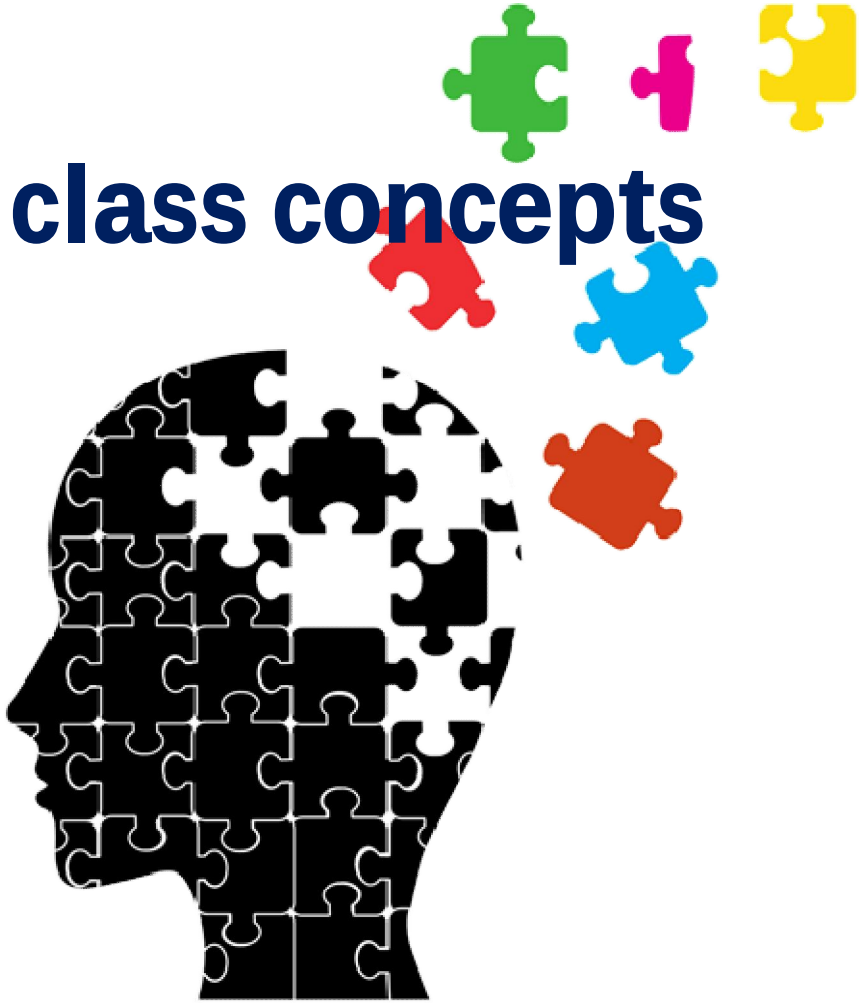
UNIT I
BASIC STRUCTURE OF COMPUTERS

Functional units – Basic operational concepts – Bus Structures – Performance – Memory locations and addresses – Memory operations – Instruction and Instruction sequencing – Addressing modes – Assembly language – **Case study : RISC and CISC Architecture.**

Recall the previous class concepts



Broad Classification

Computer architectures have evolved over the years.

– Features that were developed for **mainframes and supercomputers** in the 1960s and 1970s have started to **appear on a regular basis** on later generation microprocessors.

Two broad classifications of ISA:

a)Complex Instruction Set Computer (CISC)

b)Reduced Instruction Set Computer (RISC)

CISC versus RISC Architectures

Complex Instruction Set Computer (CISC)

–More traditional approach.

–**Main features:**

- Complex instruction set
- Large number of addressing modes (R-R, R-M, M-M, indexed, indirect, etc.)
- Special-purpose registers and Flags (sign, zero, carry, overflow, etc.)
- Variable-length instructions / Complex instruction encoding
- Ease of mapping high-level language statements to machine instructions
- Instruction decoding / control unit design more complex
- Pipeline implementation quite complex

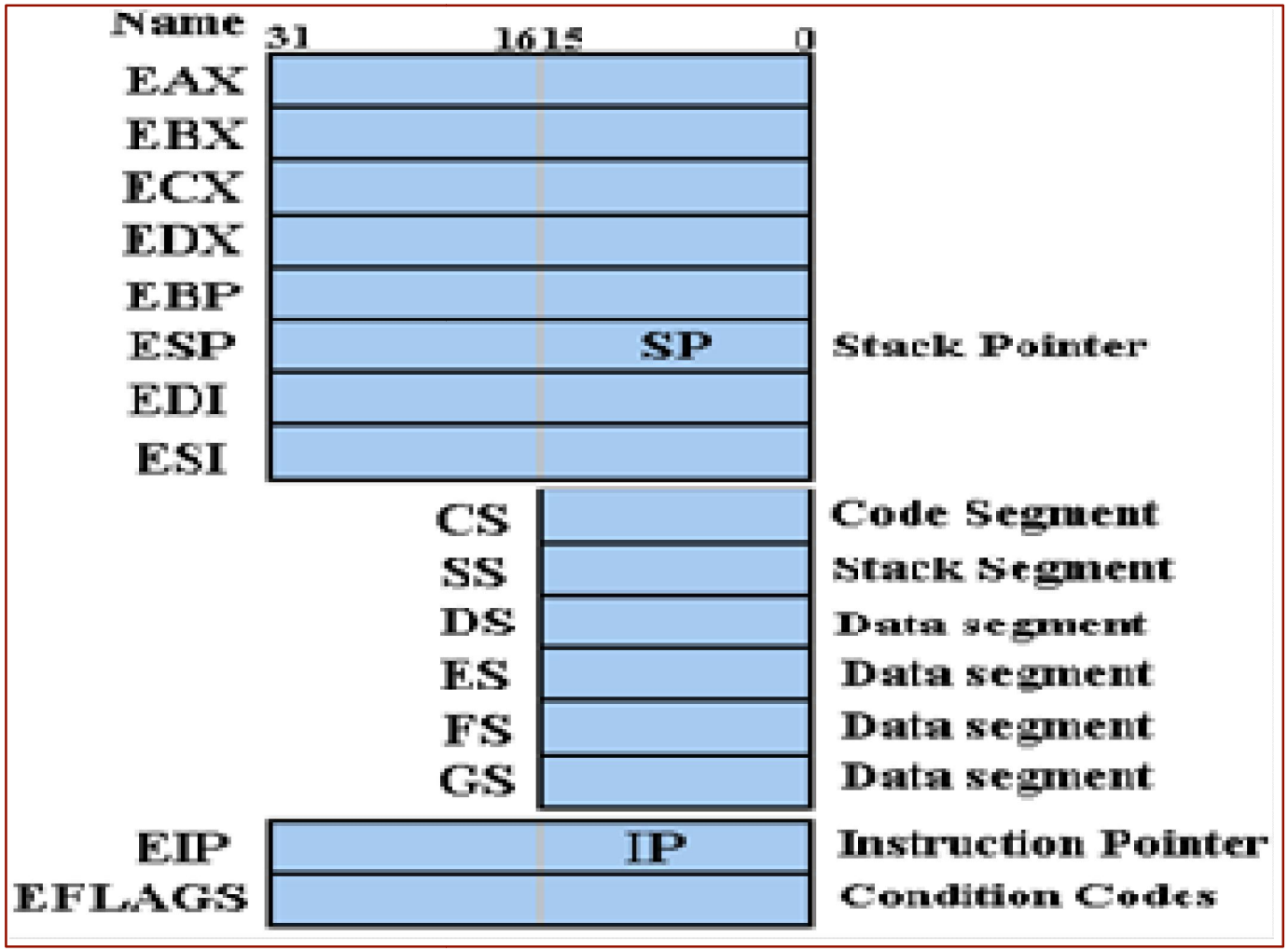
CISC Examples

- IBM 360/370 (1960-70)
- VAX-11/780 (1970-80)
- Intel x86 / Pentium (1985-present)

Only CISC instruction set that survived over generations.

- Desktop PC's / Laptops use these.
- The volume of chips manufactured is so high that there is enough motivation to pay the extra design cost.
- Sufficient hardware resources available today to translate from CISC to RISC internally.

Register Set in Pentium



Addressing Modes in VAX

Addressing Mode	Example	Micro-operation
Register direct	ADD R1,R2	R1 = R1 + R2
Immediate	ADD R1,#15	R1 = R1 + 15
Displacement	ADD R1,220(R5)	R1 = R1 + Mem[220+R5]
Register indirect	ADD R1,(R3)	R1 = R1 + Mem[R3]
Indexed	ADD R1,(R2+R3)	R1 = R1 + Mem[R2+R3]
Direct	ADD R1, (1000)	R1 = R1 + Mem[1000]
Memory indirect	ADD R1,@(R4)	R1 = R1 + Mem[Mem[R4]]
Autoincrement	ADD R1,(R2)+	R1 = R1 + Mem[R2]; R2++
Autodecrement	ADD R1,(R2)-	R1 = R1 + Mem[R2]; R2--
Scaled	ADD R1,50(R2)[R3]	R1 = R1 + Mem[50+R2+R3*d]

Reduced Instruction Set Computer (RISC)

–Very widely used among many manufacturers today.

–Also referred to as *Load-Store Architecture*.

- Only **LOAD and STORE** instructions access memory.
- All other instructions operate on processor registers.

–**Main features:**

- Simple architecture for the sake of **efficient pipelining**.
- Simple instruction set with very few addressing modes.
- Large number of general-purpose registers; very few special-purpose.
- Instruction length and encoding uniform for easy instruction decoding.
- Compiler assisted scheduling of pipeline for improved performance.

RISC Examples:

CDC 6600 (1964)

MIPS family (1980-90)

SPARC

ARM microcontroller family

- Almost all the computers today use a RISC based pipeline for efficient implementation.
  - RISC based computers use compilers to translate into RISC instructions.
  - CISC based computers (e.g. x86) use hardware to translate into RISC instructions.

Results of a Comparative Study

- A quantitative comparison of VAX 8700 (a CISC machine) and MIPS M2000 (a RISC machine) with comparable organizations was carried out in 1991.
- **Some findings:**
  - MIPS required execution of about twice the number of instructions as compared to VAX.
  - Cycles Per Instructions (CPI) for VAX was about six times larger than that of MIPS.
  - Hence, MIPS had three times the performance of VAX.
  - Also, much less hardware is required to build MIPS as compared to VAX.

Conclusion

– Persisting with CISC architecture is too costly, both in terms of hardware cost and also performance.

– VAX was replaced by ALPHA (a RISC processor) by Digital Equipment Corporation (DEC).

– CISC architecture based on x86 is different.

- Because of huge number of installed base, backward compatibility of machine code is very important from commercial point of view.
- They have adopted a balanced view: (a) user's view is a CISC instruction set, (b) hardware translates every CISC instruction into an equivalent set of RISC instructions internally, (c) an instruction pipeline executes the RISC instructions efficiently.

TEXT BOOK

Carl Hamacher, Zvonko Vranesic and Safwat Zaky, “Computer Organization”, McGraw-Hill, 6th Edition 2012.

REFERENCES

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2. William Stallings, “Computer Organization and Architecture designing for Performance”, Pearson Education 8th Edition, 2010
3. John P.Hayes, “Computer Architecture and Organization”, McGraw Hill, 3rd Edition, 2002
4. M. Morris R. Mano “Computer System Architecture” 3rd Edition 2007
5. David A. Patterson “Computer Architecture: A Quantitative Approach”, Morgan Kaufmann; 5th edition 2011

THANK YOU