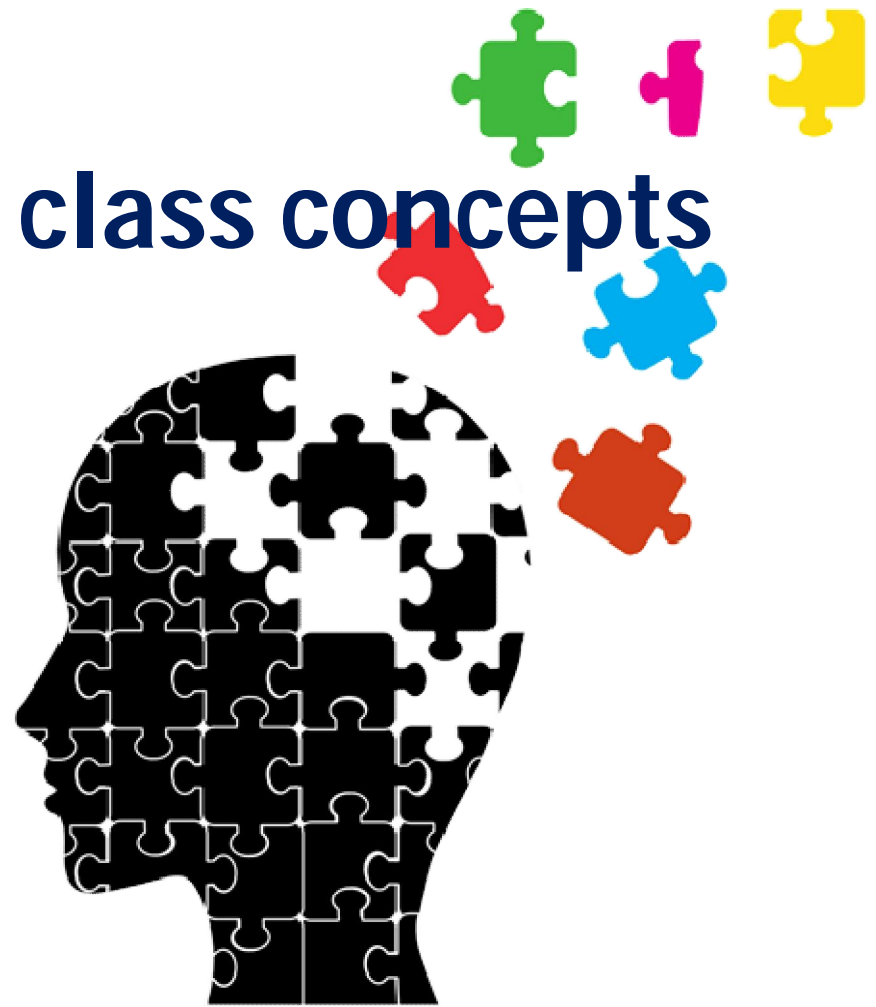# UNIT I
BASIC STRUCTURE OF COMPUTERS

Functional units – Basic operational concepts – Bus Structures – Performance – Memory locations and addresses – Memory operations – Instruction and Instruction sequencing –– Addressing modes – Assembly Language – Case study : RISC and CISC Architecture.
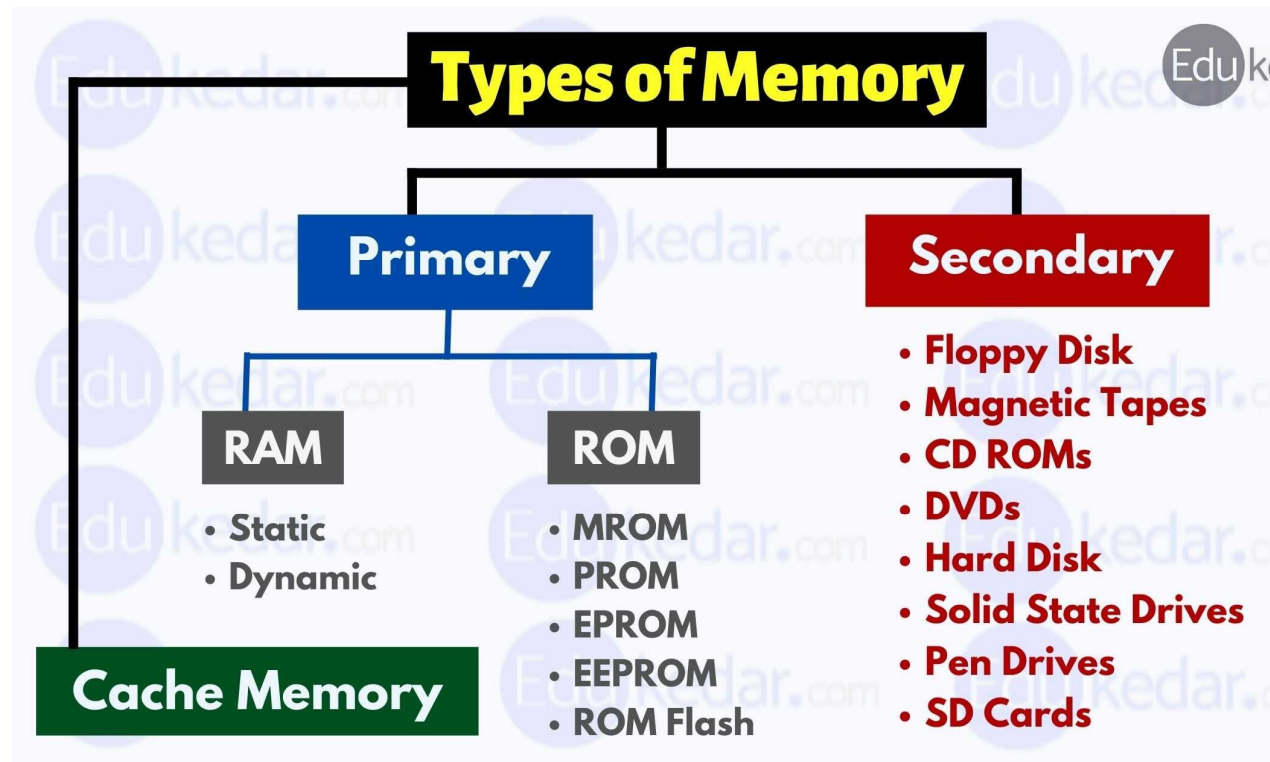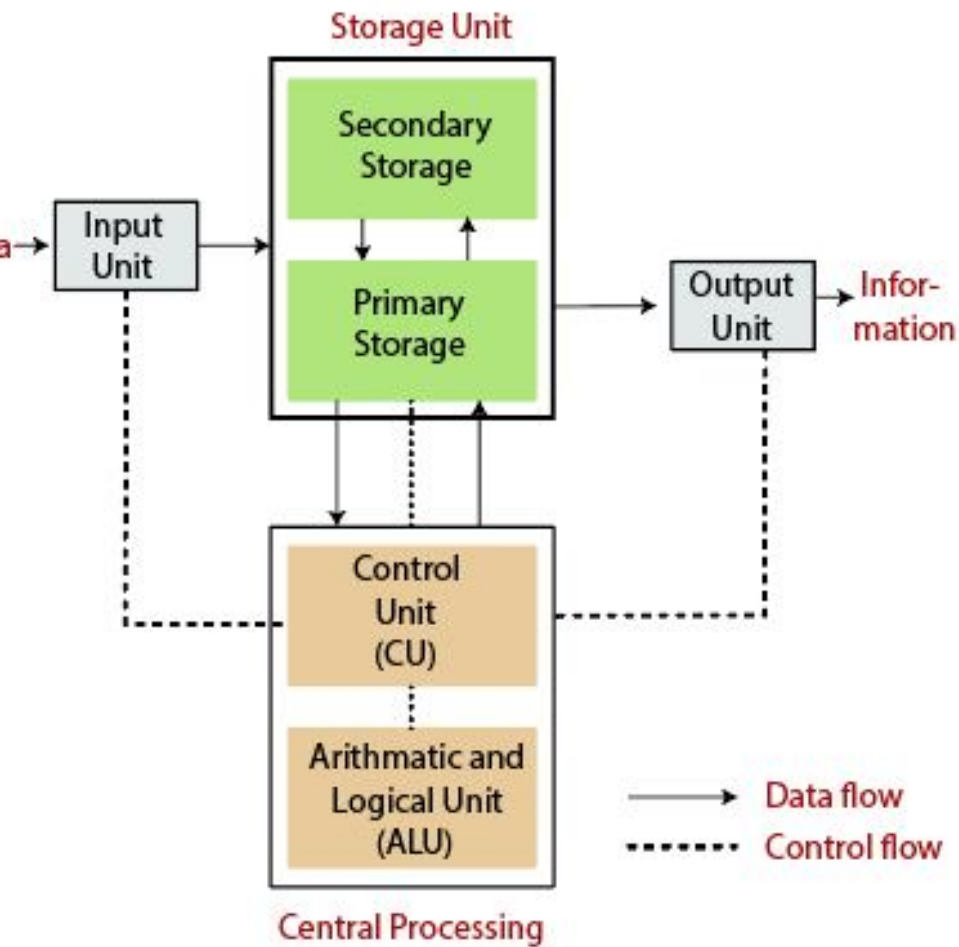
Recall the previous class concepts

Functional Unit

Block diagram of Computer

Storage Unit

Secondary Storage

Input Unit

Primary Storage

Output Unit → Information

Control Unit (CU)

Arithmatic and Logical Unit (ALU)

→ Data flow

······► Control flow

Central Processing

Types of Memory

Primary

Secondary

RAM
- Static
- Dynamic

ROM
- MROM
- PROM
- EPROM
- EEPROM
- ROM Flash

Cache Memory

- Floppy Disk
- Magnetic Tapes
- CD ROMs
- DVDs
- Hard Disk
- Solid State Drives
- Pen Drives
- SD Cards

# Analysing how processor and memory are connected

- Processors have various registers to perform various functions

- **Program Counter** - It contains the memory address of next instruction to be fetched.

- **Instruction Register** - It holds the instruction which is currently being executed

- **MDR** - It facilities communication with memory. It contains the data to be written into or read out of the addressed location.

- **MAR** - It holds the address of the location that is to be accessed

  n general purpose registers that is R0 to Rn-1

Connection between Processor & Memory
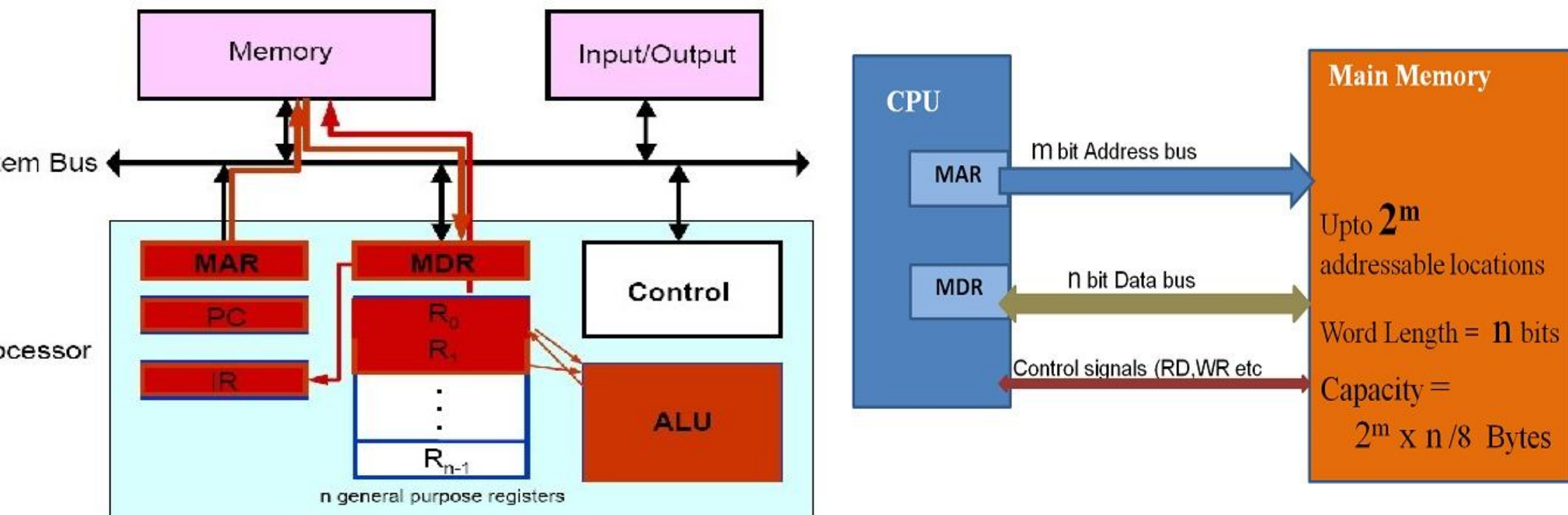
Basic Operational Concepts

- Instruction consists of 2 parts

OPCODE	OPERANDS
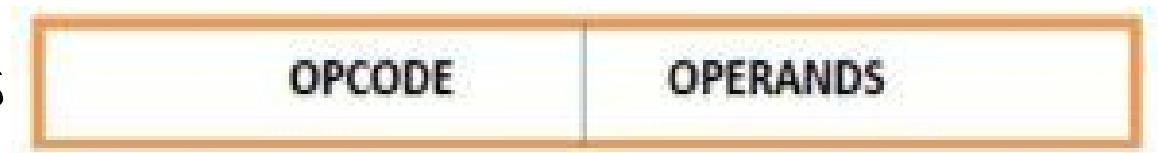
- Example

ADD   LOCA, R0

Load LOCA, R1
Add R1, R0

Instructions Format

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

op	rs	rt	constant or address
6 bits	5 bits	5 bits	16 bits

op	Target Address
6 bits	26 bits

Instructions Format

	op	rs	rt	rd	sh	fn
	31	25	20	15	10	5	0

R

6 bits	5 bits	5 bits	5 bits	5 bits	6 bits
Opcode	Source 1 or base	Source 2 or dest'n	Destination	Unused	Opcode ext

I

imm — Operand / Offset, 16 bits

J

jta — Jump target address, 26 bits

inst — Instruction, 32 bits
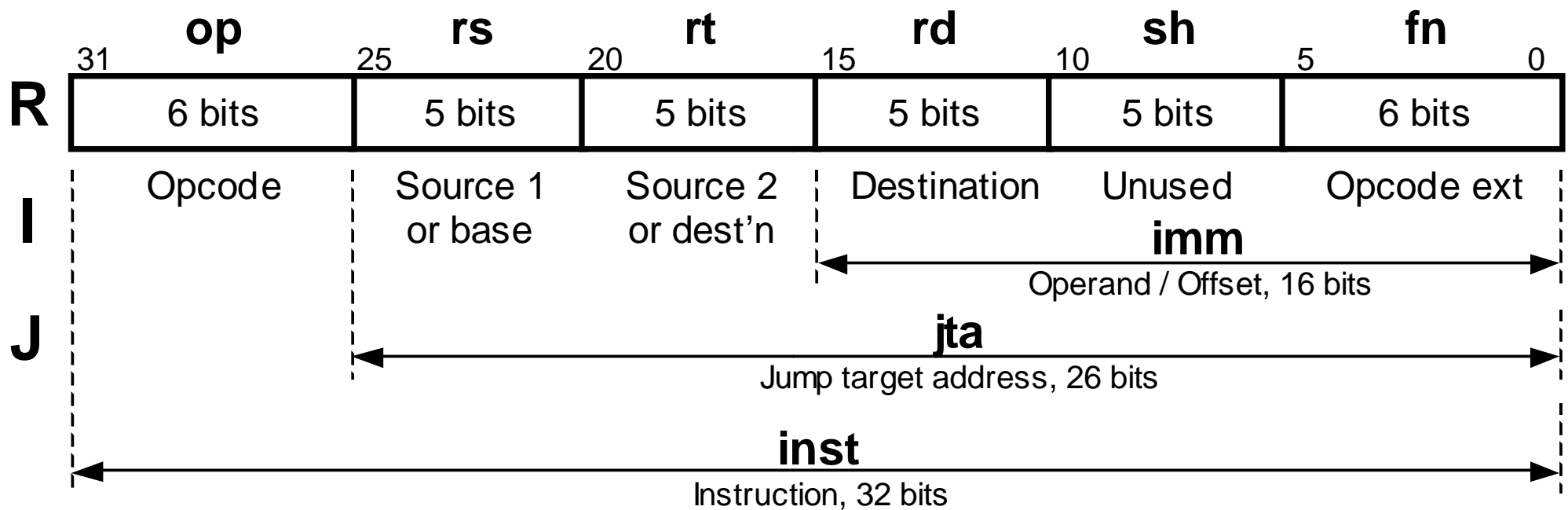
Translating Arm Assembly Instructions into Machine Instructions

op	rs	rt	rd	shamt	funct
6 bits	5 bits	5 bits	5 bits	5 bits	6 bits

add $t0, $s1, $s2

special	$s1	$s2	$t0	0	add

0	17	18	8	0	32

000000	10001	10010	01000	00000	100000

$00000010001100100100000000100000_2 = 02324020_{16}$

Operating System

TEXT BOOK

Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "Computer Organization", McGraw-Hill, 6th Edition 2012.

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2. William Stallings, "Computer Organization and Architecture designing for Performance", Pearson Education 8th Edition, 2010

3. John P.Hayes, "Computer Architecture and Organization", McGraw Hill, 3rd Edition, 2002

4. M. Morris R. Mano "Computer System Architecture" 3rd Edition 2007

5. David A. Patterson "Computer Architecture: A Quantitative Approach", Morgan Kaufmann; 5th edition 2011

THANK YOU