SNS COLLEGE OF ENGINEERING

(Autonomous)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL PRINCIPLES AND SYSTEM DESIGN

Guess Today's Topic????

Master-Slave Flipflops

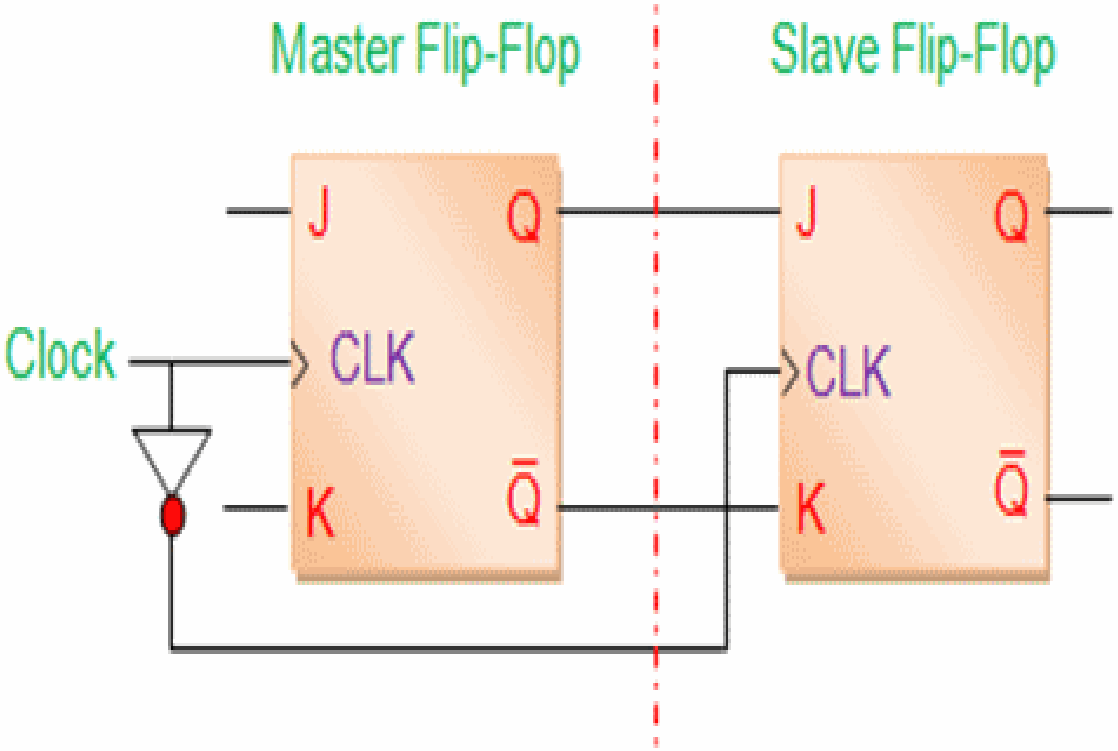


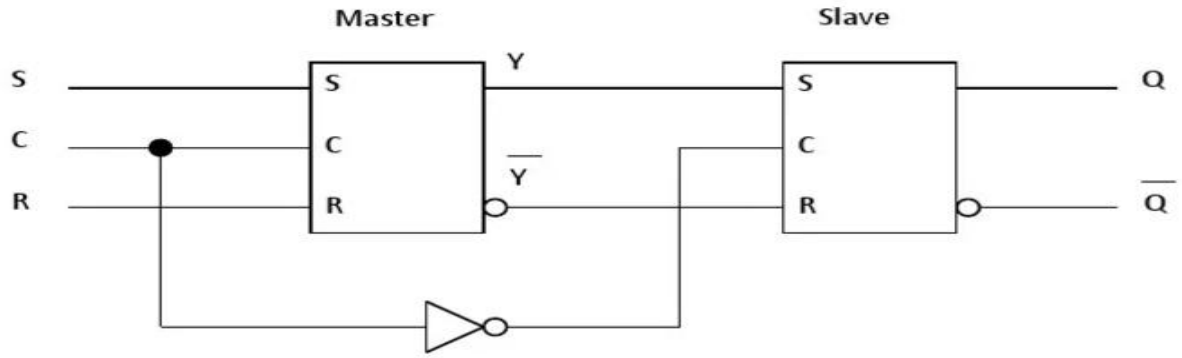
Fig 1 : Logic Diagram Master Slave Flip Flop

Master slave Flip Flop

- A master-slave flip-flop is constructed from two flip-flops.
- One circuit serves as a master and the other as a slave, and the overall circuit is referred taps a master-slave flip-flop.

SR Master-Slave Flip-Flop

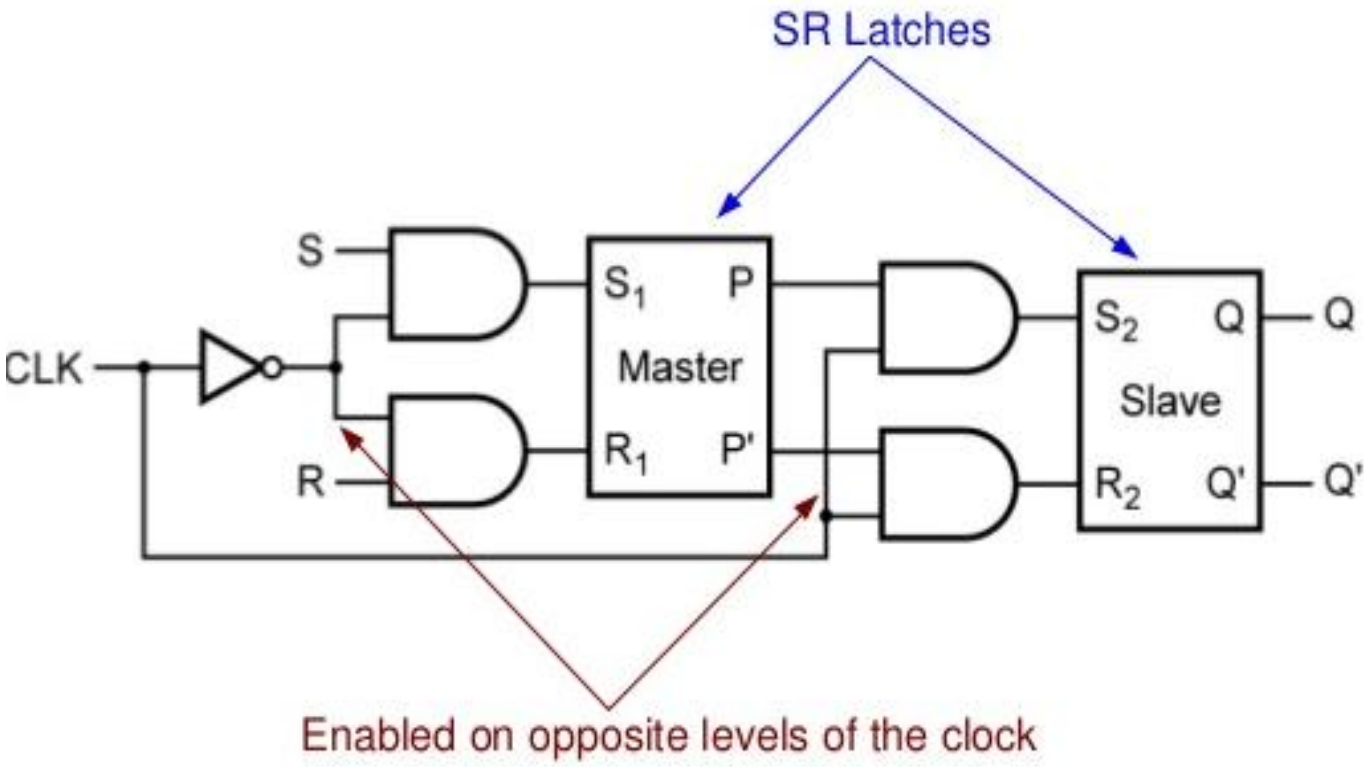
- Read input at first half of clock cycle
- Output only changed at second half of clock cycle



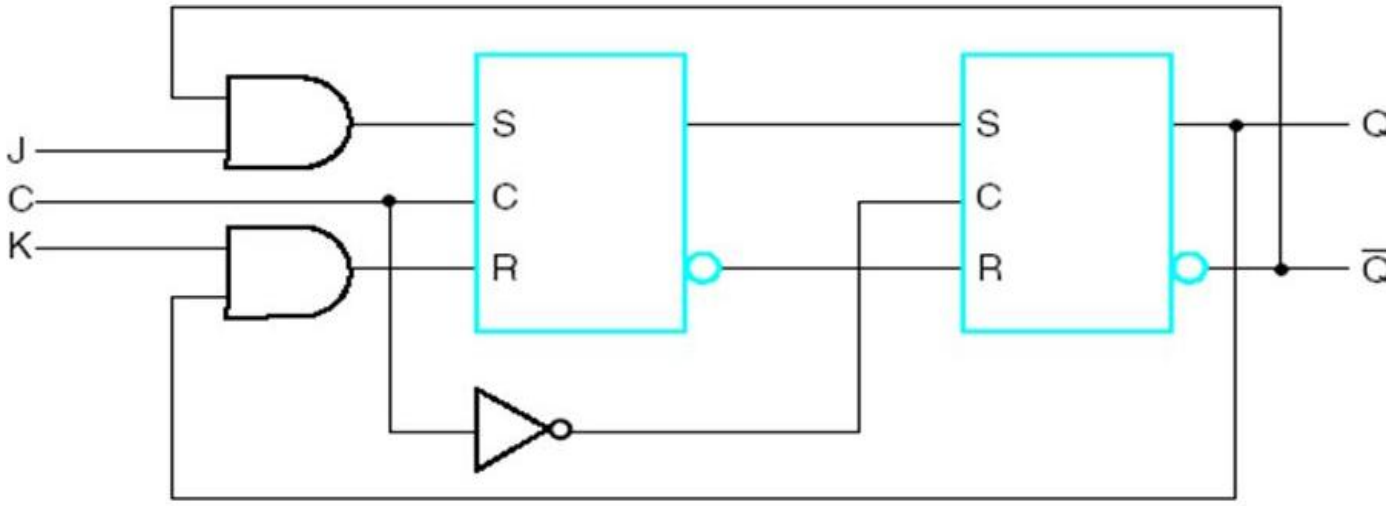
SR Master-Slave Flip-Flop

- An RS Master-Slave Flip-Flop is pulse-triggered.
- This means:
  - Data are entered on the rising edge of the clock pulse
  - But, output is only changed on the falling edge of the clock pulse

SR Flip-Flop (master-slave)



Master-Slave JK Flip-Flop



(a)

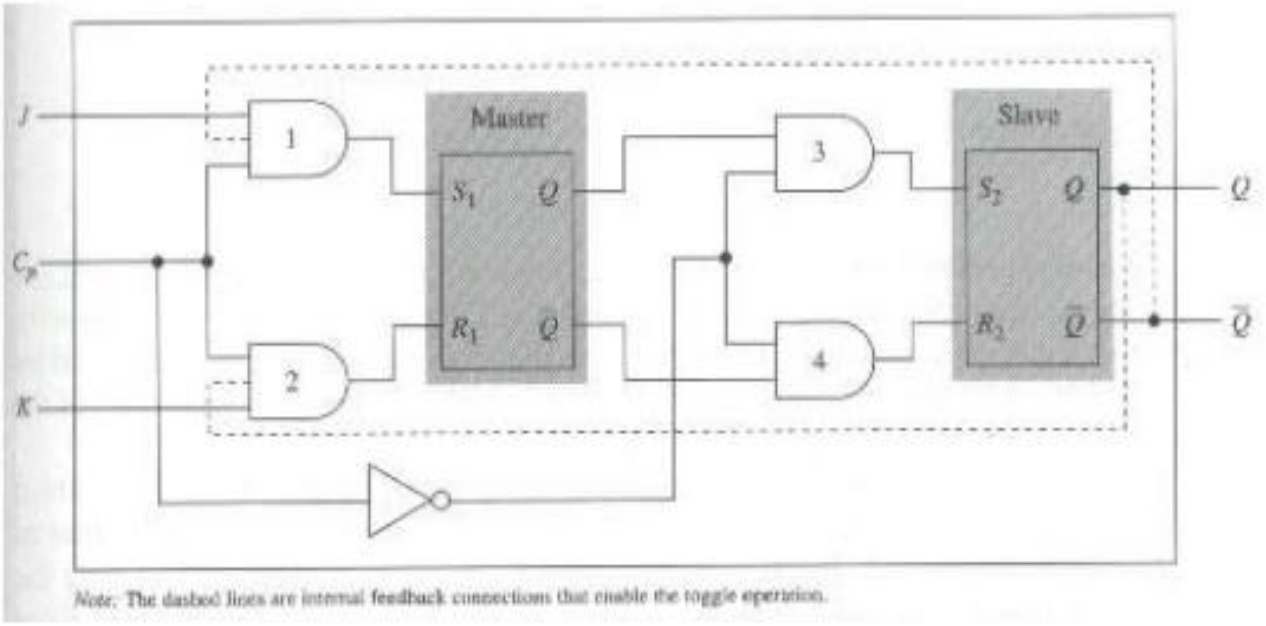
J	K	Next State of Q
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

Master-Slave J-K Flip-Flop

A master-slave flip-flop contains two flip-flops/latches:

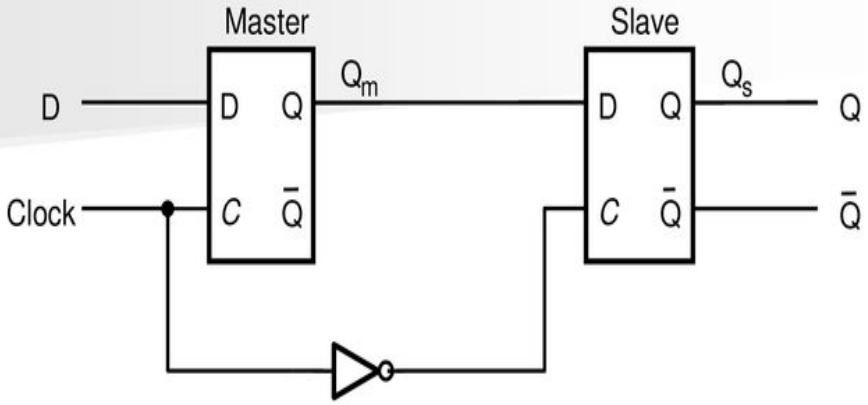
Master S-C latch (S-C Flip-Flop) - receives data while the input trigger clock is HIGH.

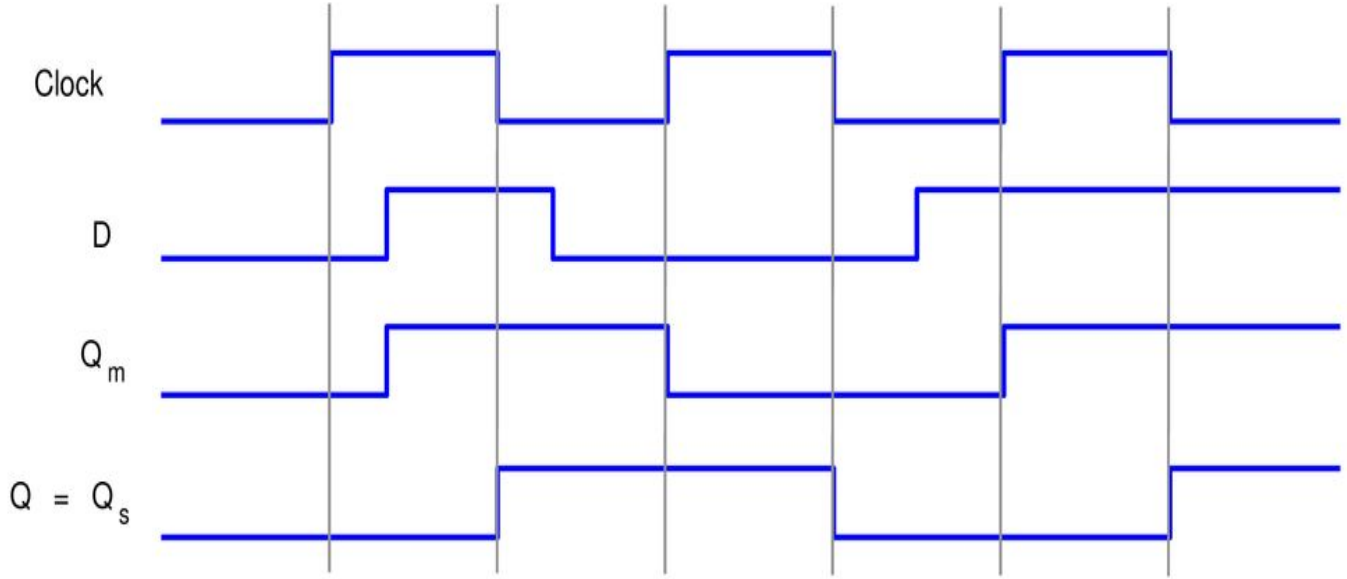
Slave S-C latch (S-C Flip-Flop) - receives data from the master and output it when the clock goes LOW.



Note: The dashed lines are internal feedback connections that enable the toggle operation.

Master-Slave D Flip-Flop





Draw the Logic diagram and Circuit diagram for Master-Slave D Flip Flop


Thank
you