

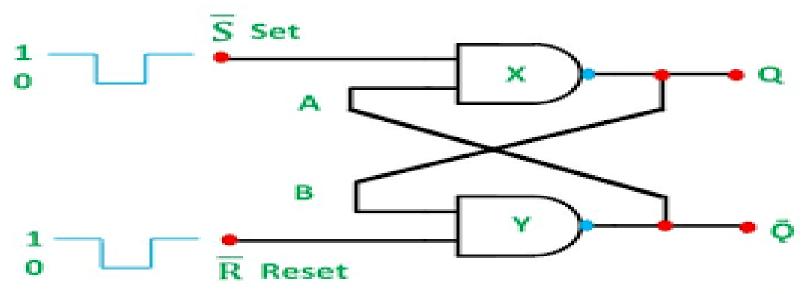
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL CIRCUITS

Guess Today's Topic????



Circuit Globe

E.DIVYA., AP/ECE / 19EC306-DIGITAL CIRCUITS/ Unit 3/ SR FlipFlop



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What is Flip flop

>>In digital circuits, the flip-flop, is a kind of bi-stable multivibrator.

>>It is a Sequential Circuits / an electronic circuit which has two stable states and thereby is capable of serving as one bit of memory , bit 1 or bit 0





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Introduction : Types Of Flip Flop

1. SR Flip Flop

a.SR Flip Flop Active Low = NAND gates b. SR Flip Flop Active High = NOR gates

- 2. Clocked SR Flip Flop
- 3. JK Flip Flop
- 4. T Flip Flop
- 5. D Flip Flop
- 6. Master-Slave Edge-Triggered Flip-Flop





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No change

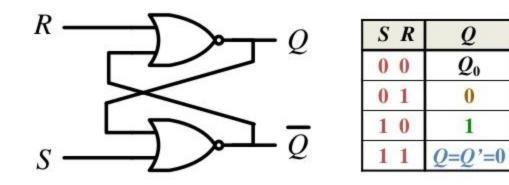
Reset

Invalid

Set

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SR Flip Flop - NOR GATE LATCH





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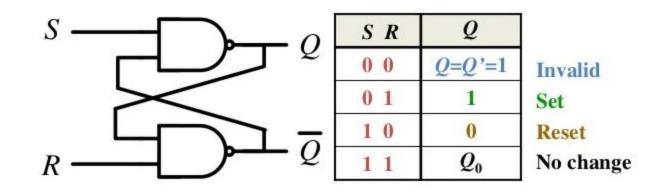


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SR Flip Flop - NAND GATE LATCH





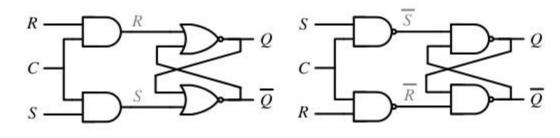
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Clocked SR Flip Flop



CSR	Q
0 x x	Q_0
100	Q_0
101	0
1 1 0	1
111	Q=Q'

No change No change Reset Set

Invalid





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SR Flip Flop - NOR GATE LATCH

STATUS	ā	Q	R	S
HOLD (NoChange)	Q	Q	0	0
RESET	1	0	1	0
SET	1 0		0	1
INVALID	0	0	1	1





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Clocked SR Flip Flop

- Additional clock input is added to change the SR flip- flop from an element used in asynchronous sequential circuits to one, which can be used in synchronous circuits.
- The clocked SR flip flop logic symbol that is triggered by the PGT is shown in Figure.
- Its means that the flip flop can change the output states only when clock signal makes a transition from LOW to HIGH.





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Clocked RS Flip Flop

clock	S	R	Q	ā	STATUS
1	0	0	Q	a	HOLD (NoChange)
1	0	1	0	1	RESET
Ť	1	0	1	0	SET
1	1	1	0	0	INVALID





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Clocked SR Flip Flop

