



# **SNS COLLEGE OF ENGINEERING**



**Kurumbapalayam(Po), Coimbatore - 641 107**

**Accredited by NAAC-UGC with 'A' Grade**

**Approved by AICTE, Recognized by UGC & Affiliated to Anna University, Chennai**

## **Department of Information Technology**

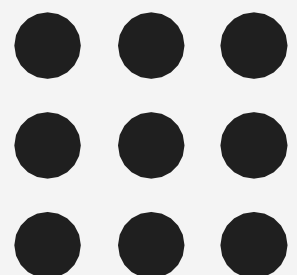
**Course Name - 19IT301 Computer Organization and  
Aechitecture**

**II Year / III Semester**

**Unit 1 - Basic Structures of Computers**

**Topic :Instructions and Instructions Sequencing**

**19IT301 / UNIT 1/Instruction and instruction  
Sequencess/K.Sangeetha/ECE/SNSCE**





# Using Registers



- Registers are faster
- Shorter instructions

The number of registers is smaller (e.g. 32 registers need 5 bits)

- Potential speedup
- Minimize the frequency with which data is moved back and forth between the memory and processor registers.

# BRANCHING

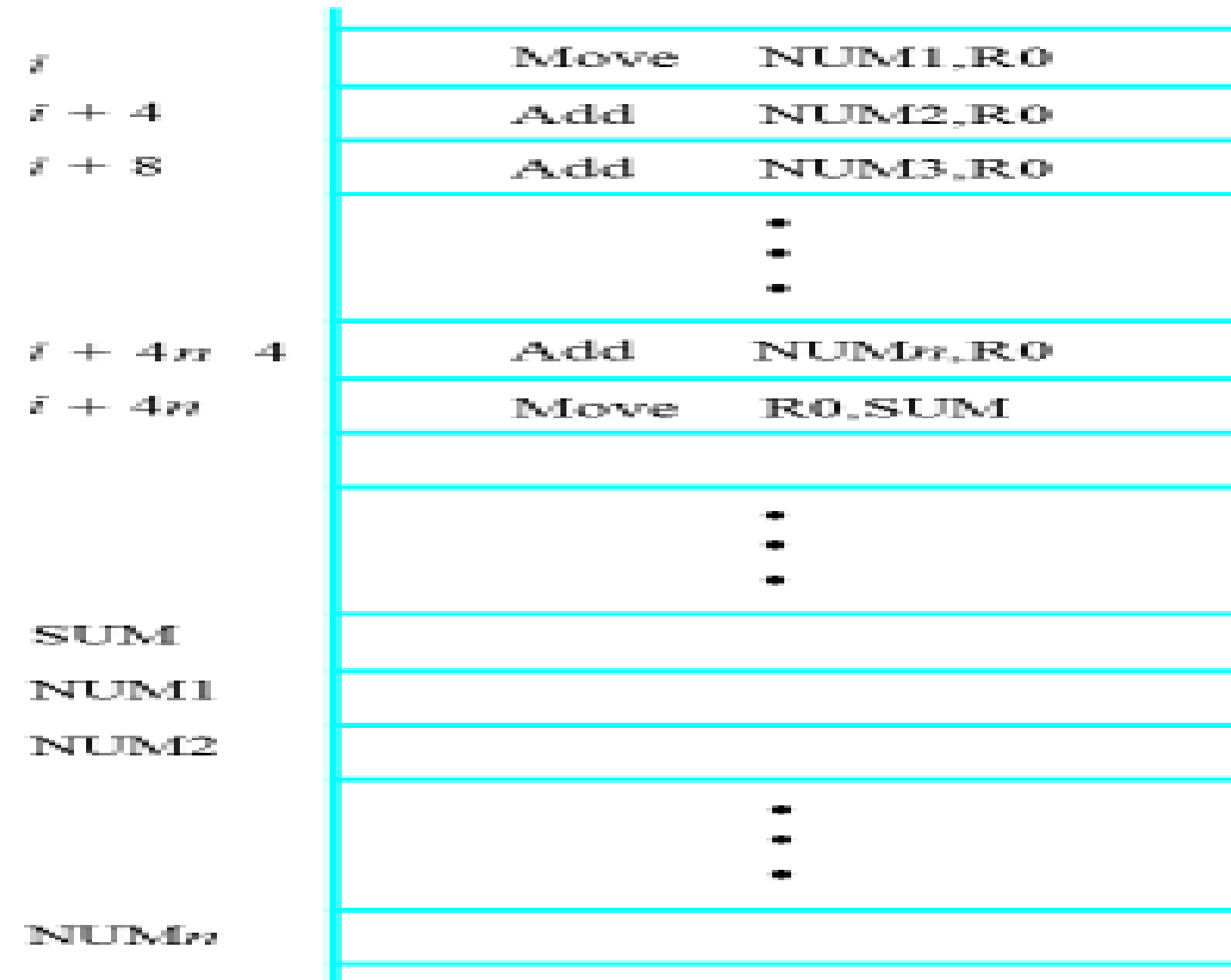


Figure 2.9. A straightline program for adding  $n$  numbers.

# BRANCHING

$i$	Move	NUM1,R0
$i + 4$	Add	NUM2,R0
$i + 8$	Add	NUM3,R0
		⋮
$i + 4n - 4$	Add	NUM $n$ ,R0
$i + 4n$	Move	R0,SUM
		⋮
SUM		
NUM1		
NUM2		
		⋮
NUM $n$		

Figure 2.9. A straightline program for adding  $n$  integers

# Instruction

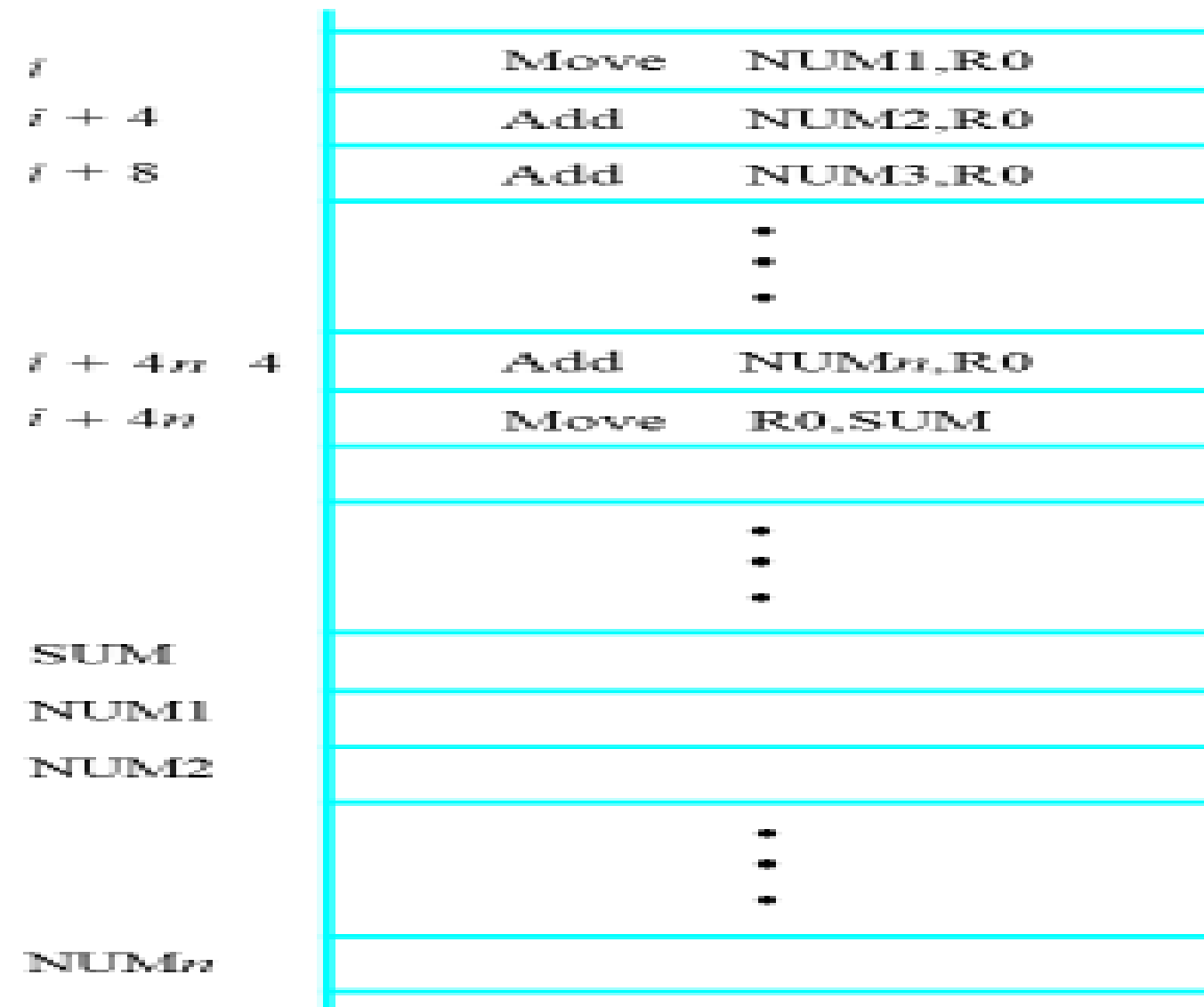


Figure 2.9. A straightline program for adding  $n$  numbers.



# Condition Codes



- Condition code flags
- Condition code register / status register
- N (negative)
- Z (zero)
- V (overflow)
- C (carry)
- Different instructions affect different flags



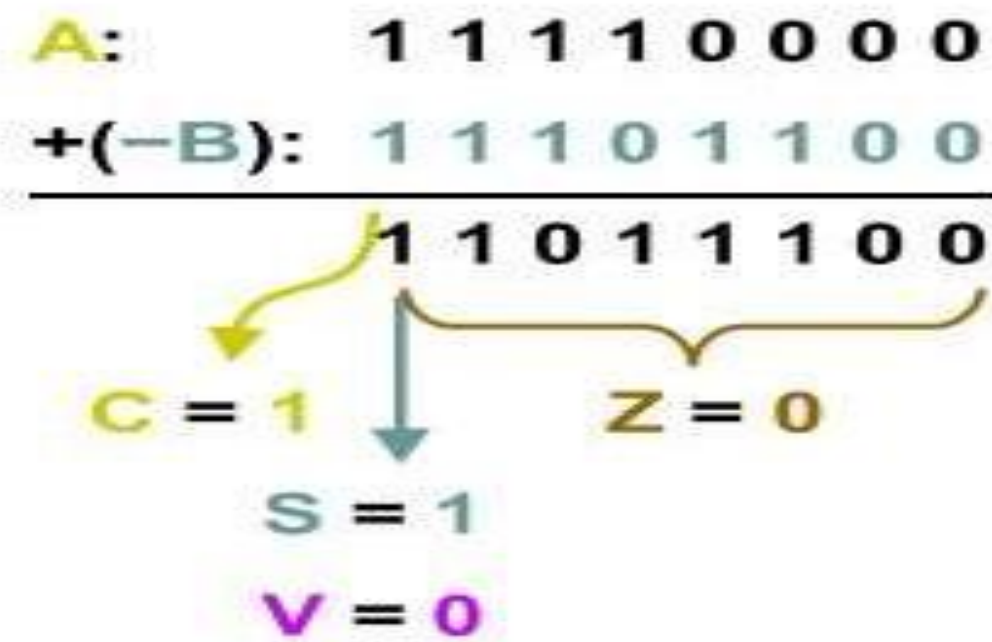
Instruction



## Conditional Branch Instructions

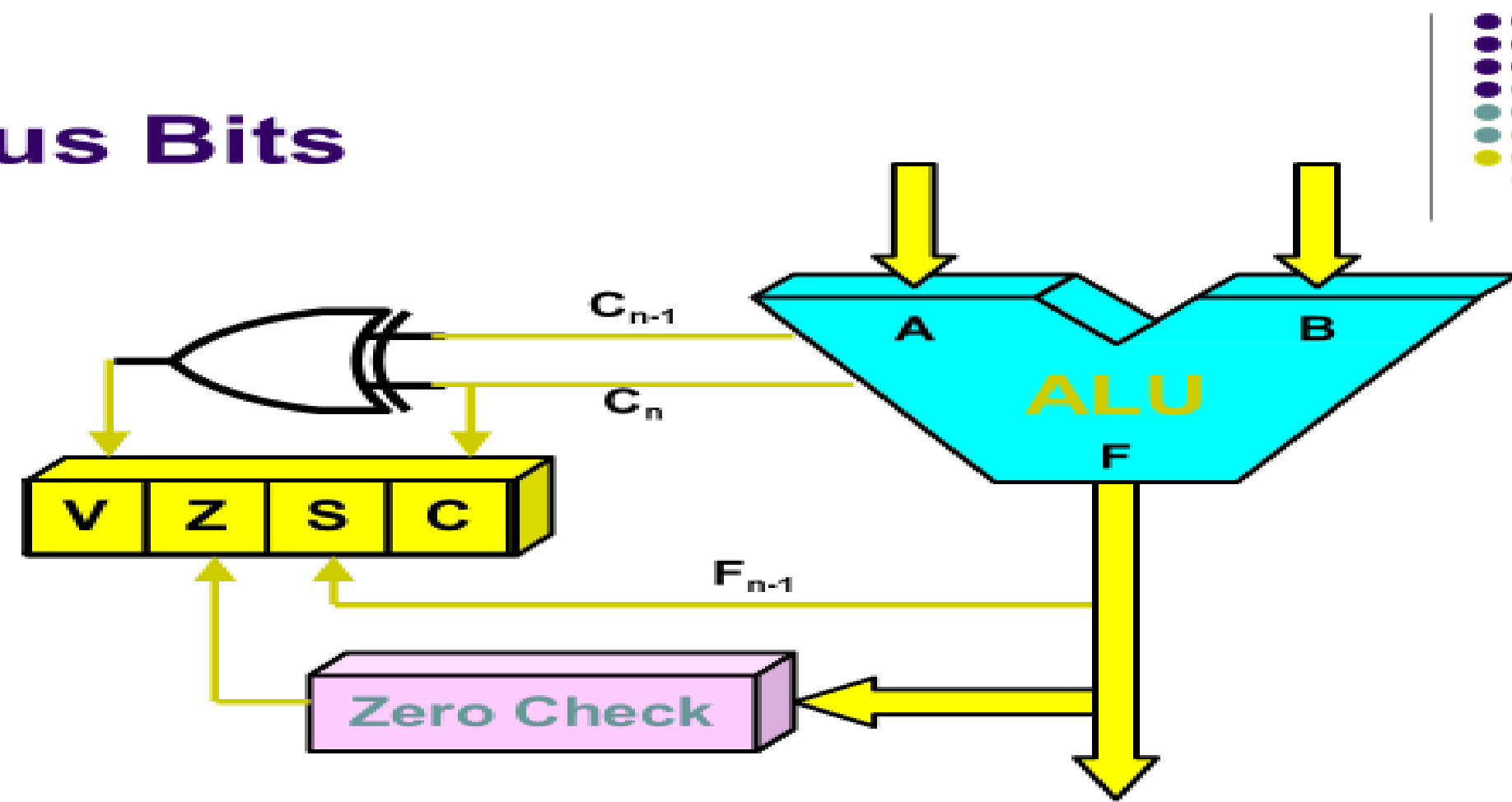
- Example:

- A: 1 1 1 1 0 0 0 0
- B: 0 0 0 1 0 1 0 0



Instruction

## Status Bits







**THANK YOU**